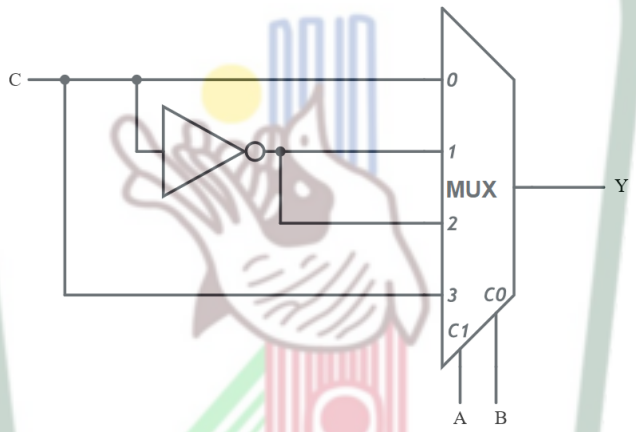
DIGITAL ELECTRONICS (UIE403)
End-Term Examination-2025
Full Marks- 100
Answer Question No.1 and any four from the rest

Q1: a) Answer the following questions- 10 X 2 = (20)

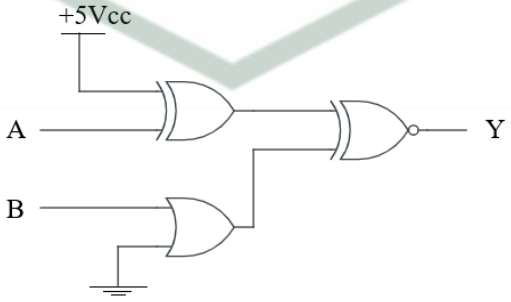
i) $(\ )_7 = (25)_{10} = (\ )_5$
ii) Product-of-sum expression for AND gate is-
iii) Addition of 2's complement of a binary number 'X' to a binary number $(1100)_2$ results in $(1000)_2$ with a carry. Find X.
iv) For a Hex-to-seven-segment-display decoder, if the input in binary is $(1111)_2$, the output bits for (a,b,c,d,e,f,g) will be _____.
v) If all the inputs of a 4:1 MUX are tied to logic '1', then the expression for the output Y is _____.
vi) For a high priority octal-to-binary encoder, if the input stream is $(01100111)_2$, the output is ____.
vii) If both the inputs of an edge triggered J-K flip-flop are permanently tied to logic '1', what will be its output state after the 4th clock pulse if the present output before the application of clock input is 1.
viii) Modulus of a counter is defined as _____.
ix) Number of address lines required for a 2048 X 8-bit memory chip is _____.
x) If the present state of a J-K flip-flop is 1, then the inputs required at J&K to retain the output are __.

Q2: a) For the logic circuit given below, answer the following questions-



i) Find out the expression and truth table for Y. 2 + 2 = (4)
ii) Identify the function achieved by the given circuit. (2)
iii) What needs to be done in the circuit to make the output expression Y = A? (2)

b) For the logic circuit diagram given below, answer the following questions-



i) Find out the expression and truth table for Y. 2 + 2 = (4)
ii) Minimize the output expression. (2)

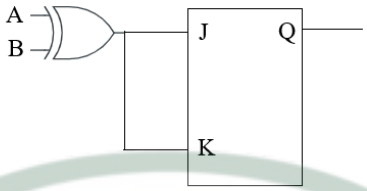
c) Explain the working of a 4-bit binary adder with the help of proper functional block diagram. (6)

Q3: a) Explain the working of an Active HIGH J-K flip-flop with Preset and Clear inputs. (5)

b) It is required to design a digital keypad with six switches named as S0, S1, S2, S3, S4, S5 that will produce the binary equivalent of the switch's numbers corresponding to a HIGH input from each of these switches. Determine the truth table and draw the logic circuit with basic gates. (5)

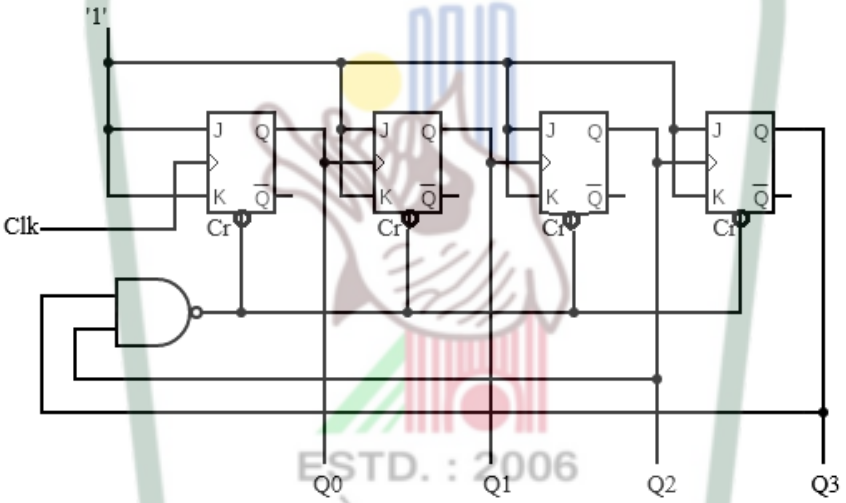
c) Design a MOD-5 asynchronous UP counter that resets itself after the last stable state. (6)

d) Find out the characteristic table and the characteristic equation for the J-K flip-flop configured as below in terms of A and B inputs. (4)



Q4: a) Implement a T-flip flop with a J-K flip-flop. (4)

b) Assuming the counter is reset initially and configured as below, answer the following questions-



i) Is the counter shown above synchronous or asynchronous? (1)
ii) Draw the timing diagram of Q3, Q2, Q1 & Q0 for at least six clock pulses. (4)
iii) State whether the counter is an UP counter or a DOWN counter. (1)
iv) What is the modulus of the counter? (2)
v) Write down the whole sequence of the counter with Q3 as MSB and Q0 as LSB. (3)
vi) If the clock frequency is 2 KHz, what will be the frequencies of Q3 and Q2? (2)
vii) What will be the modulus of the counter if Q1 replaces Q2 at the input of the NAND gate? (2)
viii) What can be done to reverse the sequence of the counter above? (1)

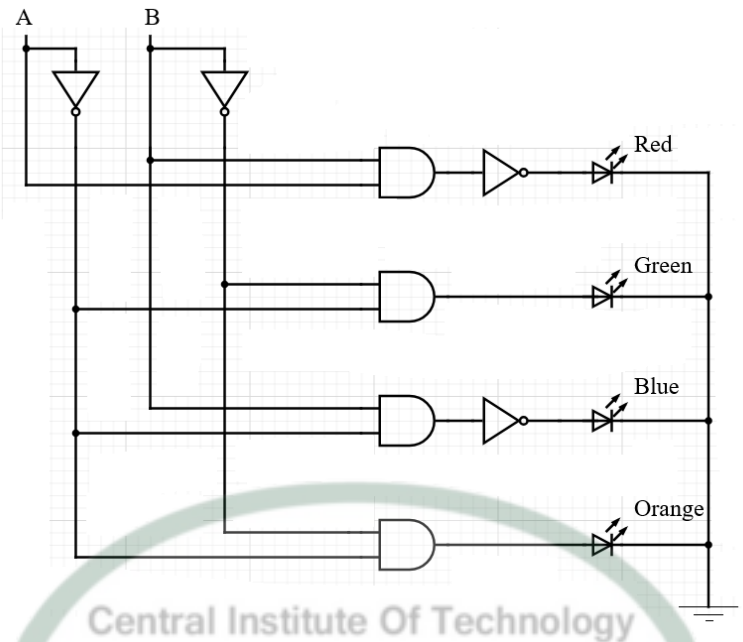
Q5: a) With a suitable PLA, implement a full-adder circuit. (6)

b) Design a counter that will have the following sequence- (6)

0-4-2-5-7-0

c) State two differences between a Combinational circuit and a Sequential circuit. (2)

d) For the diagram given below, answer the following questions-



i) Which of the LEDs will be turned ON if A = B = 0? (2)
ii) What inputs should be applied at A & B to turn ON only the RED LED? (2)
iii) What inputs should be applied at A & B to turn ON only the BLUE LED? (2)

Q6: a) Implement the Boolean function $Y(A,B,C) = \sum m(0,2,5,6)$ with the help of a 4:1 MUX and few additional gates. (4)

b) Draw the logic circuit diagram of an Active-LOW S-R latch with NAND gates and state its characteristic table. Also, derive the excitation table of the latch from the characteristic table. 4 + 2 = (6)

c) A memory chip is built with 256 registers with each register capable of storing 4 bits.

i) What is the size of the memory chip in bytes? (1)
ii) How many address lines will be required to address these registers? (1)
iii) What will be the address of the first and the last registers in Hex? (2)
iv) How many such chips will be required to build a 1 Kbyte memory system? (2)

d) Consider a three-input Ex-OR gate where A and B are two of the inputs and the third input is permanently tied to logic '1'. Find out the truth table. (2)

e) Implement an Ex-NOR gate using NAND gates only. (2)