Total number of printed pages: 03 **B. Tech (UG)/4th Sem /UIE403**

2024

DIGITAL ELECTRONICS

Full Marks: 100

Time: Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. a) i) Hexadecimal Number that comes before A000 (H) and after A9FF (H) are- 10 x 2=20

ii) Addition of 1's complement of an 8-bit number Y to another number (00001001), results in a 9-bit number (100000011). Find Y.

iii) The output of a 4-input Ex-NOR gate is _____ when the number of inputs that are HIGH is even.

iv) $(\_\_\_)_7 = (25)_{10} = (\_\_\_)_6$

v) Minimum number of half adders required to add two 8-bit data is-

vi) If the number of input lines in a Multiplexer is 36, then the minimum number of select lines required is-

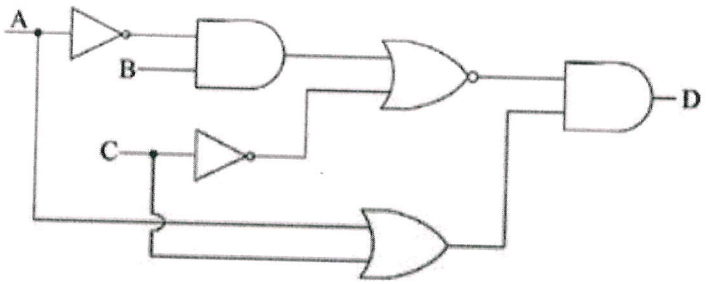
vii) In a five variable K-Map, a group having eight elements/squares will result in a term having ____ variables.

viii) In a 3-bit asynchronous UP-counter with outputs Q2, Q1, Q0, the output Q2 is connected via a NOT gate to the Clear inputs of all the flip-flops. How many stable states will the counter have?

ix) For an active HIGH edge triggered J-K flip-flop, the inputs J and K are permanently tied to logic '1'. What will be the output of the flip-flop in the third clock pulse if the present output is LOW?

x) It is required to design a Counter capable of counting up to 2000 items. How many flip-flops will be required?

2. a) Find the output expression for D and derive the truth table and minimize the expression if possible. 5



b) Minimize the Boolean function- $(A.B + A.\bar{B})(\bar{A} + A.B.C + \bar{B}.C)$ 2

c) Implement Ex-OR and EX-NOR gates by using only NOR gates. 2+2 = 4

d) Minimize using K-Map technique- 4+5 = 9

i) F (A,B,C,D) = ∑m(0,1,4,5,7,8,12,13) + ∑d(3,10,15)

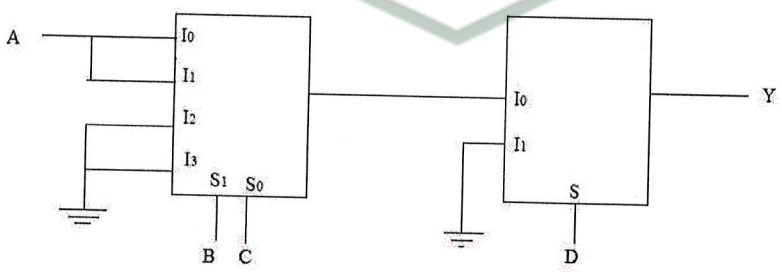
ii) F (A,B,C,D,E) = ∑m(1,6,7,8,9,15,16,19,29,30,31) + ∑d(0,1,5,20,28)

3. a) Explain the working of a full-adder circuit with proper diagram and truth table. 5

b) Explain the working of a 1-bit Magnitude Comparator circuit with the help of its truth table and logic diagram. 5

c) Implement the Boolean function Y (A,B,C) = ∑m(1,2,5,6) with a 4:1 MUX and few additional gates. 6

d) Find out the expression for Y- 4



4. a) Implement a Full-subtractor with a 3-to-8-line Decoder and few additional gates. 5

b) Construct an Active-LOW S-R latch with NAND gates and find out the characteristic equation of the output from its characteristic table. 5

c) Differentiate between Level triggered flip-flops and Edge triggered flip-flops. 2

d) For an edge triggered J-K flip-flop with Preset and Clear inputs, find out the status of Q_{n+1} immediately after it is clocked for the following four conditions. (Assume Q_n=0). 4

i) J = 0, K = 0, Pr = 1, Cr = 1

ii) J = 1, K = 0, Pr = 1, Cr = 1

iii) J = 0, K = 0, Pr = 1, Cr = 0

iv) J = 0, K = 1, Pr = 0, Cr = 1

e) A 100 kHz clock signal is applied to a J-K flip-flop with J = K = 1. Determine the frequency of Q_{n+1} and find out the time required by the flip-flop to produce five number of HIGH outputs. 4

5. a) Implement a D-flip-flop using a J-K flip-flop. 6

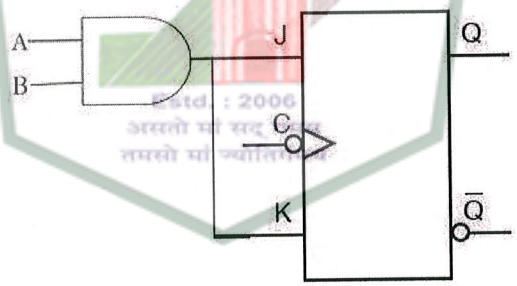
b) Design a modulo-5 asynchronous DOWN counter. 6

c) Design a synchronous counter that has the following sequence- 8

000->010->101->110->100->111->000

6. a) Explain the working of a 4-bit storage Register. 6

b) For the J-K flip-flop shown in the diagram below, find out the Characteristic Table and Transition Table in terms of the input variables A and B. 6



c) Implement a 3-bit binary-to-gray converter circuit with the help of a suitable PLA. 8