Total number of printed pages = 6

19/4th Sem/UIE 403

2022

DIGITAL ELECTRONICS

Full Marks – 100

Time – Three hours

The figures in the margin indicate full marks for the questions.

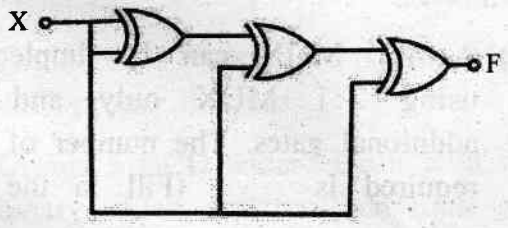
Answer any *five* questions.

1. (i) Hexadecimal Number that comes after F9FFh is ____. (Fill in the blank) 2×10=20

   (ii) Addition of 1's complement of a number Y to a number X, yields ____. (Fill in the blank)

   (iii) The output of a 2-input gate is always LOW when one of its inputs is permanently tied to logic 1. The gate is ____. (Fill in the blank)

   (iv) Expression for F is ____. (Fill in the blank)



[Turn over

(v) Minimum number of half adders required to add two 8-bit data is _____. (Fill in the blank)

(vi) If the number of input lines in a Multiplexer is N, then the number of select lines required is _____. (Fill in the blank)

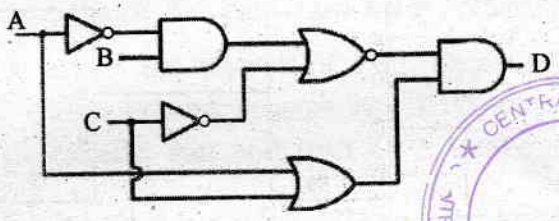
(vii) In a five variable K-Map, a group having eight elements/squares results in a term having _____. (Fill in the blank)

(viii) In a 3-bit asynchronous counter with outputs Q2, Q1, Q0, the output Q1 is connected via a NOT gate to the Clear inputs of all the flip-flops. How many stable states will the counter have ?

(ix) For an active HIGH edge triggered J-K flip-flop, the current input is J=0 and K=1. What will be the output in the next state if both the inputs are given HIGH inputs ?

(x) A 4:1 MUX can be implemented by using 2:1 MUX only and with no additional gates. The number of 2:1 MUX required is ____. (Fill in the blank)

2. (a) Find the output expression for D and derive the truth table and minimize the expression if possible. 5



(b) Minimize the Boolean function : 2

$(A.B + A.\bar{B})(\bar{A}+A.B.C+\bar{B}.C)$

(c) Implement Ex-OR and Ex-NOR gates by using only NOR gates. 2+2=4

(d) Minimize using K-Map technique 4+5=9

(i) $F(A,B,C,D) = \sum m(0,1,4,5,7,8,12,13) + \sum d(3,10,15)$

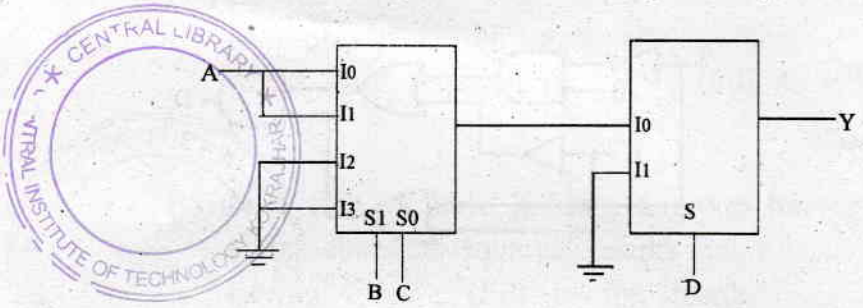
(ii) $F(A,B,C,D,E) = \sum m(1,6,7,8,9,15,16, 19,29,30,31) + \sum d(0,1,5,20,28)$

3. (a) Explain the working of a full-adder circuit with proper diagrams. 4

(b) Design a BCD adder circuit with two 4-bit binary adders and few additional gates. 6

(c) Implement the Boolean function Y(A,B,C,D) = Σm(1,5,6,8,9,12,15) with 8:1 MUX. 6

(d) Find out the expression for Y 4



4. (a) Implement a Full-subtractor with a 3-to-8 line Decoder and few additional gates. 5

(b) Explain the working of an Active-LOW S-R latch. 5

(c) Differentiate between Level triggered flip-flops and Edge triggered flip-flops. 2

(d) A smart room has two fans— one exhaust fan (E) and one intake fan (I) which are controlled depending on the inputs that its circuit gets from four sensors namely, Temperature sensor (T), Humidity sensor (H),

Pressure sensor (P) and CO_2 sensor. The fans are controlled based on the following conditions : 8

(i) when the output of both Humidity and Pressure sensors is HIGH, turn ON exhaust fan and turn OFF intake fan.

(ii) when the output of both Pressure and Temperature sensors is HIGH, turn ON exhaust fan and turn OFF intake fan.

(iii) when the output of Pressure sensor is LOW, turn OFF exhaust fan and turn ON intake fan.

(iv) when the output of CO_2 sensor is HIGH, turn ON both fans.

(v) for any unspecified condition that may arise, turn ON both fans.

Find out the truth table and implement the logic circuit with as minimum number of gates as possible.

5. (a) Implement a D-flip-flop using a J-K flip-flop. 6

(b) Design a modulo-5 asynchronous DOWN counter. 6

(c) Design a synchronous counter that has the following sequence :

$000 \rightarrow 010 \rightarrow 101 \rightarrow 110 \rightarrow 100 \rightarrow 111 \rightarrow 000$ 8

6. (a) Explain the working of TTL based NAND gate with its circuit diagram. 6

(b) Explain the working of a PROM with proper logic diagram. 6

(c) Implement a 3-bit binary to gray converter circuit with the help of a suitable PLA. 8