Total number of printed pages: 7 **Programme(UG)/Semester/UIE302**

2022

Electronic Devices and Circuits

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1.	a)	Derive the expression for density of states function of a cubic crystal with lattice constant 'a'.	10
	b)	Derive the expression for thermal equilibrium electron concentration in the conduction band of an N-type semiconductor	10
2	a)	Derive the expression for Fermi Dirac distribution function.	10
	b)	Define Fermi level and explain how Fermi level is positioned in intrinsic, N-type and P-type semiconductor.	5
	c)	Derive the Einstein's equation for diffusion.	5
3.	a)	Derive the built-in potential expression of a p-n junction under zero bias.	10
	c)	Derive the expression for depletion width of a p-n junction under zero bias.	10
3.	a)	Explain the working of half wave and fullwave rectifiers with neat diagram	8
	b)	Draw the circuit diagram and output waveforms of Positive simple series clipper and Positive biased series clipper	6
	c)	Given the load line of Fig. 1 and the defined Q -point, determine the required values of V_{CC} , R_C , and R_B for a fixed-bias configuration.	6

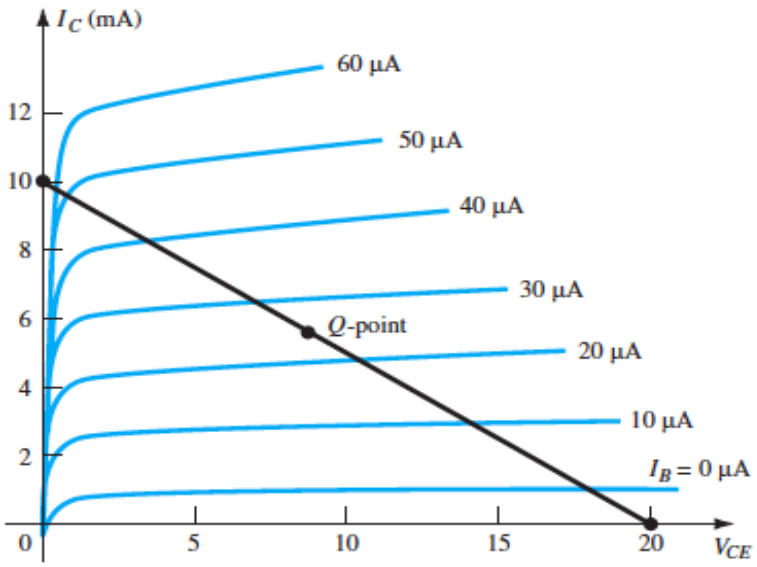
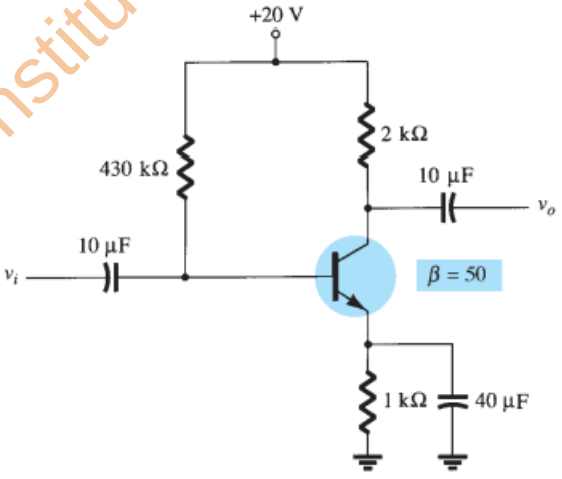


Fig. 1

4.	a)	For the emitter-bias network of Fig. 2 , determine: a. I_B . b. I_C . c. V_{CE} . d. V_C . e. V_E . f. V_B . g. V_{BC} .  Fig.2	14
	b)	Determine the dc bias voltage V_{CE} and the current I_C for the voltagedivider configuration of Fig. 3 .	6

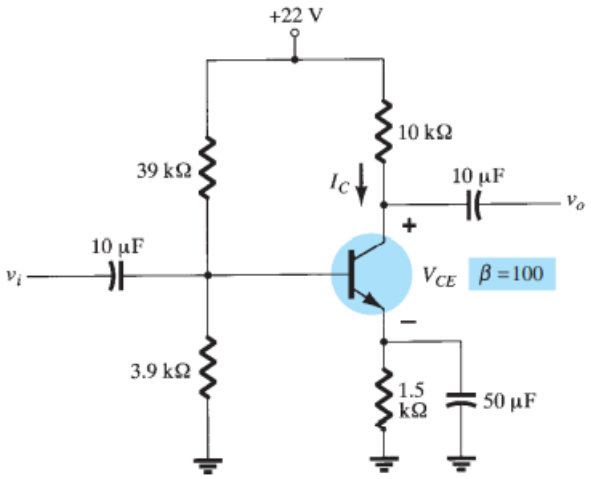
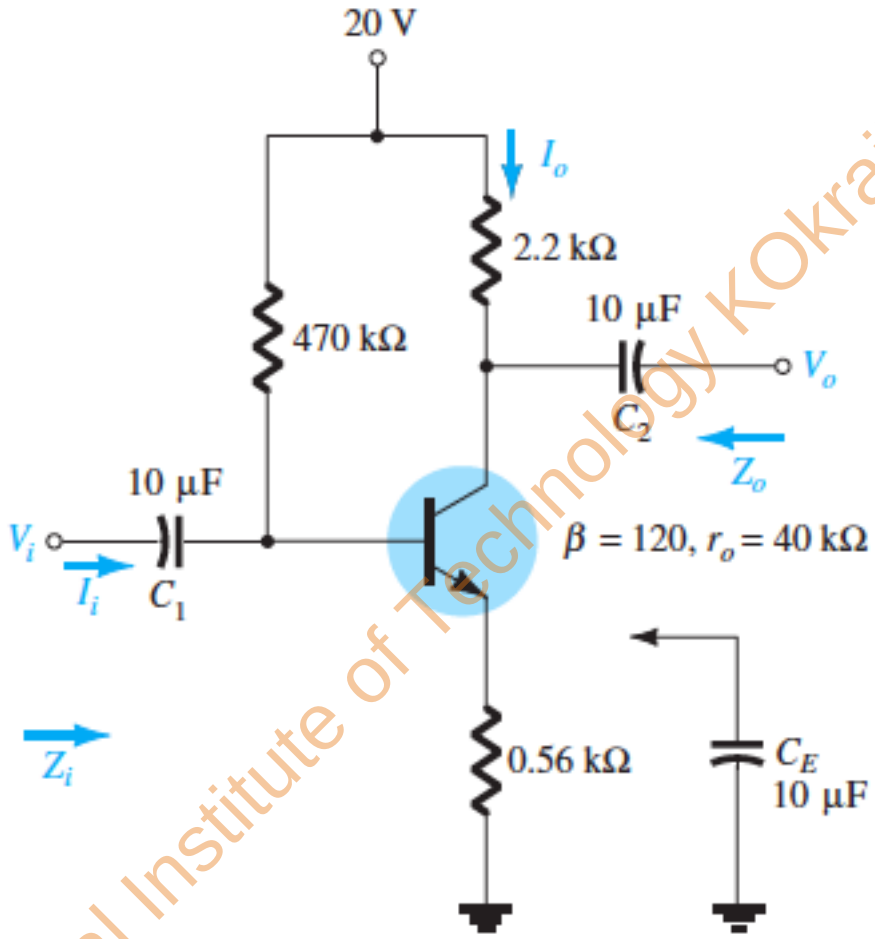
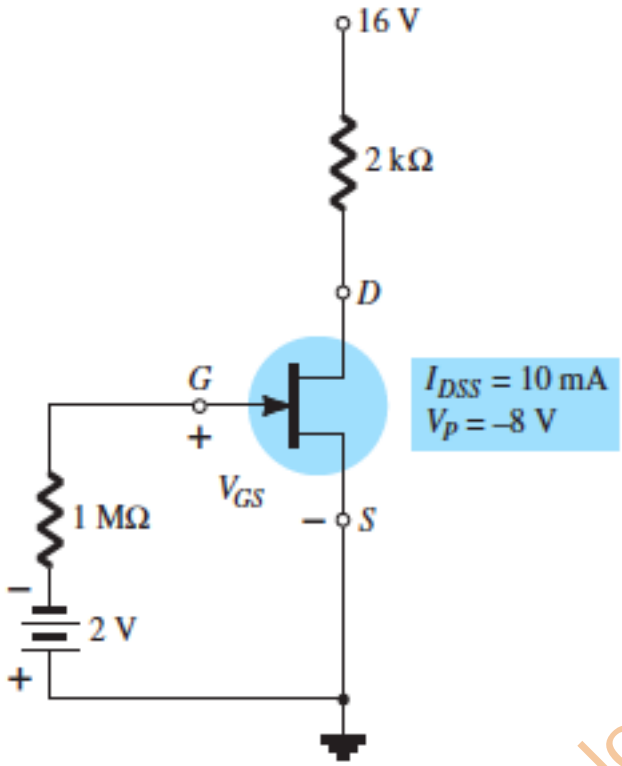
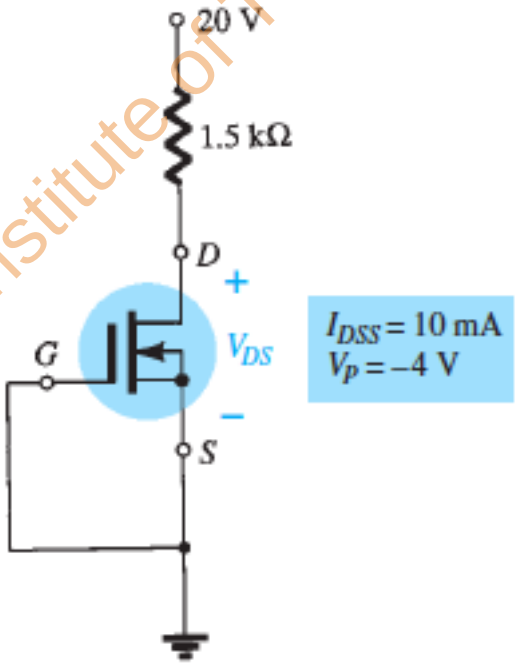


Fig. 3

5	a)	Derive the expressions for input impedance, output impedance and voltage gain of Common Emitter fixed bias and voltage divider bias configurations	14

	b)	For the network of Fig. 4 , without C_E (unbypassed), determine: a. r_e . b. Z_i . c. Z_o . d. A_v .  Fig. 4	6
6.	a)	Determine the following for the network of Fig. 5: a. V_{GSQ}. b. I_{DQ}. c. V_{DS} . d. V_D . e. V_G . f. V_S .	6

		 Fig. 5	
	b)	Determine V_{DS} for the network of Fig. 6.  Fig. 6	4
	c)	Explain the feedback biasing and voltage divider biasing of Enhancement type MOSFET	10
7.	a)	Derive the expressions for gain for voltage series and voltage shunt	6+6=12

		feedback	
	b)	Determine the maximum efficiency of a series fed class A amplifier	8