Total number of printed pages: 2 **BTech(UG)/6/UECE601**

2023

VLSI DESIGN

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1	a)	Find the expression for electric field in the oxide and depletion region of an ideal MOS capacitor operating in the depletion mode of operation.	6
	b)	Draw the energy band diagram of an ideal MOS structure in strong inversion mode of operation.	4
	c)	Explain how the oxide charges and body bias influence the value of threshold voltage for an NMOS transistor.	5+5
2	a)	Discuss how the following level-1 SPICE parameters are defined for a MOSFET: UO, LAMBDA, TOX, CJ, CJSW, MJ, MJSW, CGDO	10
	b)	What are the roles of PMOS and NMOS transistors in the topology of a static CMOS circuit?	4
	c)	Plot the transfer characteristics of a CMOS inverter and specify different regions of operation for both devices. Explain how noise margin can be determined from it.	6
3	a)	Evaluate the value of t_{pHL} of a CMOS inverter by computing the time to discharge the output capacitance from V_{DD} to $0.5V_{DD}$.	10
	b)	Find the expression for different power dissipation mechanisms in a CMOS inverter.	10
4	a)	Draw the RC model for a 3-input NAND gate and evaluate its fall time using Elmore delay model.	8
	b)	Explain how various transistors in a CMOS NAND3 gate are sized. Draw the stick diagram and layout for this gate indicating color codes.	4+8
5	a)	A unit inverter with input capacitance 3C needs to drive a capacitive load of 6000C. Find the optimum number of inverter stages and their respective sizing that can minimize the path delay between the input and the output.	10
	b)	Discuss any two methods to reduce the logical effort of a logic gate with appropriate design examples.	10

6	a)	Discuss how a combinational unit can be designed to perform multiple arithmetic operations on two 4-bit numbers using a 3-bit opcode.	10
	b)	Draw the state diagram of a 3-bit sequence detector which can detect the sequences '000' and '111'. Describe the same as a Moore machine using Verilog HDL.	4+6
7	a)	Describe how the behavior of a synchronous digital system can be captured using RTL design methodology. Draw the block diagram of a 4-bit register which can STORE and LOAD 4-bit data.	4+4
	b)	With the help of an ASM chart, describe the sequence of all register transfer operations required to implement a digital system which can add or subtract two 4-bit numbers based on the state of a mode input when an active start signal is detected.	8
	c)	Draw the circuit diagram of a 1T-DRAM cell and explain the complete READ operation cycle.	4