Total number of printed pages: 2 **BTech(UG)/6/UECE601**

2024

VLSI DESIGN

Full Marks : 100

Time : Three hours

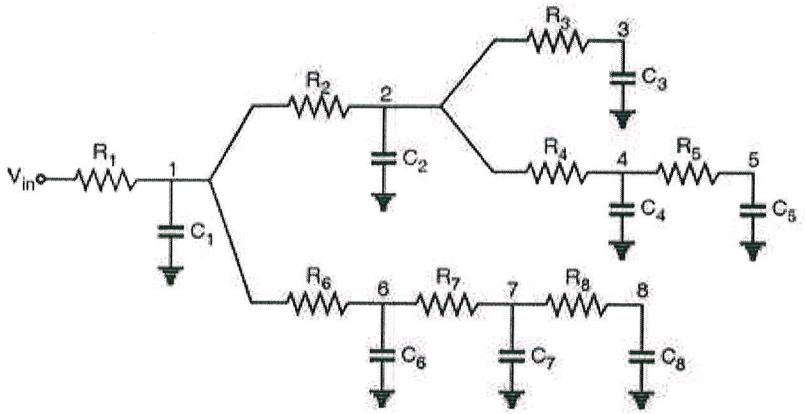
The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1.	a)	Derive the expression for drain current in a PMOS transistor. Explain how channel length modulation affects its I-V characteristic.	6
	b)	Draw and explain the energy band diagram of a MOS structure when its flat band voltage is negative.	6
	c)	Find the expression for surface potential and oxide potential in MOS structure and using them evaluate the threshold voltage of MOSFET when body bias is zero.	8
2	a)	Draw and discuss the voltage and current transfer characteristics of a CMOS inverter. Explain how noise margin is determined from it.	5
	b)	Derive the expression for trip-in (mid-point) voltage of a CMOS inverter. What is the effect of increasing $\mu_n C_{ox}(\frac{W}{L})_n$ with respect to $\mu_p C_{ox}(\frac{W}{L})_p$ on the value of trip-in voltage?	5
	c)	Explain how load capacitance influence the rise and fall time of a CMOS inverter output?	5
	d)	Derive the expression for short circuit power dissipation in a CMOS inverter.	5
3	a)	What are the different parasitic capacitors in a MOSFET operating in saturation region? Give expressions for each. Explain why the output of a CMOS inverter goes negative before charging to VDD.	8+2
	b)	Design a CMOS circuit to implement the logic function, $Y = \overline{A(B+C)+DE}$ and estimate the propagation delay of this circuit. Draw the layout for this circuit clearly indicating the color and width of different regions.	10
4	a)	Design a Moore FSM which can detect the sequence '1010' including overlapping cases. Write a Verilog program to describe the same.	5+5
	b)	What is algorithmic state machine (ASM)? Taking the example of an Add-Shift multiplier, explain how an ASM chart is utilized to implement the	2+8

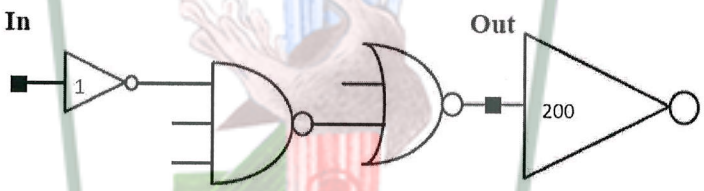
RTL design.

5 a) For the RC tree network shown below, derive the expression for time constant for node-5 assuming V_{in} to be a unit step function. 8



RC tree network

b) For the combinational circuit given below the size scaling factors of the input and output gates are given. Determine the size scaling factors of in-between gates which will minimize the path delay. Determine whether inserting additional inverters can optimize the delay further. Give reasons. 8+4



6 a) Implement a 4x1 MUX using transmission gate logic. 4

b) Compare the ASIC and FPGA based design flow. With a neat diagram explain the general architecture of an FPGA. 4+6

c) Briefly discuss the different process steps required to make a PMOS transistor on a p-type wafer. 6

7 a) Differentiate between the read and write operations of 1T and 3T DRAM cells using a neat circuit diagram and necessary signal waveforms. 8

b) What are the advantages of transmission gate logic? Draw the circuit diagram and explain how a 4x1 MUX could be implemented. 6

c) Compare the impact of constant field scaling with that of generalized scaling. 6
