Total number of printed pages: **2** **UG/3rd/UECE306**

2024

SUBJECT NAME: Digital Electronics & Logic Design

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1.	a)	Use x-or gate to realize a xor b xor c .	1
	b)	Use nand gate to realize a+b.	1
	c)	Use basic gates to realize a+b(cd').	1
	d)	Write down the truth table and symbol of a positive edge triggered D master slave flip flop.	2 +1=3
	e)	Design a 4:1 multiplexer.	6
	f)	Explain the function of a 2 bit asynchronous counter with circuit diagram, timing waveform etc	8
2.	a)	Draw the circuit of S_R latch and explain the truth table	2+2=4
	b)	Write down the truth table of a 2 bit binary to gray converter	1
	c)	Design a 1:4 de-multiplexer	5
	d)	Draw the circuit of a j-k latch	2
	e)	Convert a s-r latch into j-k latch using synthesis method	7
3.	a)	Simplify xycv+(cv)'yx+(xy)'+1'.	1
	b)	Use nor gate to realize ab.	1
	c)	Use k-map to simplify ∑m(0,4,5,9,7,14)+d(1,6,13).	5
	d)	Draw the circuit diagram of a 4 bit gray to binary converter	3
	e)	Design a Mod-3 counter using j-k mater slave flip flop	10
4.	a)	Draw and explain the state transition table of j-k flip flop	2+2=4
	b)	Plot Q output for a positive edge triggered j-k master slave flip flop for	2

		single clock pulse when j=0 and k=0		
	c)	Plot Q output for a negative edge triggered s-r master slave flip flop for two clock pulse (1st clk pulse s=1 and k=0 2nd clk pulse s=0 r=0)		2
	d)	Design a Mod-5 counter using j-k mater slave flip flop		12
5.	a)	Use k map method to simplify the following functions		4+4+2=10
		i)	F(A,B,C,D) = π [M(2,3,4,5,7,8,9,10)]	
		ii)	f(m,n,o,p) = ∑{m(1,2,3,5,7,9,10)}+d(11,12,13)	
		iii)	f(a,b,c)=ab'c+a'b'c'+abc+a'b'c	
	b)	Use Boolean algebraic techniques to simplify (xy'+x'y)'(x'+y)		1
	c)	Use basic gates to draw the logic diagram of Y= (a+b)'a'b'c without changing the function		1
	d)	Use only NOR gate to implement Y=(a+b'+c)(a+c')		2
	e)	Design a 2 bit comparator		6
6.	a)	Draw the block diagram of the following		2x2=4
		i)	4 bit SISO right shift register	
		ii)	2 bit synchronous up counter	
	b)	Why truth table can not be used to design a counter?		3
	c)	Convert the following		3
		i)	Decimal 20 to octal	
		ii)	Hexadecimal A12 into binary	
		iii)	Binary 10.01 into decimal	
	d)	Design a Mod-7 counter using j-k mater slave flip flop		10
7.	a)	State De- morgan's theorems		2
	b)	Distinguish the following		2+2=4
		i)	Sequential logic and combinational logic	
		ii)	Edge triggering and pulse triggering of latch	
	c)	Derive the characteristics equations of j-k flip flop		4
	d)	Use only NAND gate to realize Y=ab' +b'c+ca'		3
	e)	Write down the function table of the followings		1.5x2+1+3=7
		i)8:1 multiplexer ii)1:8 De-multiplexer iii) half subtractor ii) BCD to seven segment decoder		