Total number of printed pages: **2**

UG/3rd/UECE306

2023

SUBJECT NAME: Digital Logic Design

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1.	a)	Write down excitation table and truth table of j-k master slave flip flop.	2 x 2=4
	b)	Write down the main difference between the above two table.	1
	c)	Explain the excitation table and the truth table of j-k master slave flip flop.	3 x 2=6
	d)	Write down the truth table and symbol of a clocked j-k latch	2 +1=3
	e)	What is the main difference between a clocked latch and mater slave flip flop	1
	f)	Draw the block diagram of a Mater slave D flip flop and explain the function with timing diagram	1+4=4
2.	a)	Draw the circuit of i) S_R latch ii)S_R latch with enable	2
	b)	What is the function of this above enable input.	1
	c)	What do you understand by data hazard ? Explain how is that same problem is solved by using pulse triggered latch.	1+5=6
	d)	Draw the circuit of a j-k latch	2
	f)	Convert a j-k latch into s-r latch using synthesis method	9
3.	a)	Draw the block diagram of a 2 bit asynchronous counter and explain it's function with the help of timing diagram.	2+4 = 6
	b)	Explain how the synchronous function is different than asynchronous function	1
	c)	Draw the symbol and function table of a negative edge triggered D master slave Flip flop.	1+1=2
	d)	Design a Mod-6 counter using j-k positive edge triggered mater slave flip flop	11

4.	a)	Draw and explain the state transition table of j-k flip flop		2+2=4
	b)	Plot Q output for a positive edge triggered j-k master slave flip flop for single clock pulse when j=0 and k=0		2
	c)	Plot Q output for a negative edge triggered s-r master slave flip flop for two clock pulse (1^{st} clk pulse s=1 and k=0 2^{nd} clk pulse s=0 r=0)		2
	d)	Design a Mod-8 counter using j-k negative edge triggered mater slave flip flop		12
5.	a)	Use k map method to simplify the following functions		4+4+2=10
		i)	$F(A,B,C,D) = \sum m(2,5,7,8,9,10,11,12,13)$	
		ii)	$f(m,n,o,p) = \pi M(1,2,3,5,7,9,10)$	
		iii)	$f(a,b,c)=\sum m(0,1,4,5)$	
	b)	Use Boolean algebraic techniques to simplify (xy'+x'y)'(x+y)		1
	c)	Use basic gates to draw the logic diagram of Y= (a+b)'a'b'c without changing the function		1
	d)	Use only NOR gate to implement Y=(a+b'+c)(a+c')		2
	e)	Design a 2 bit comparator		6
6.	a)	Draw the block diagram of the following		2x2=4
		i)	3 bit SISO right shift register	
		ii)	2 bit synchronous down counter	
	b)	Use basic gates to draw Y= xyz'+x'y'z+x'y'z'+x'yz'		3
	c)	Convert the following		3
		i)	Decimal 67 to octal	
		ii)	Hexadecimal F12 into binary	
		iii)	Binary 11.01 into decimal	
	d)	Convert a s-r latch into j-k latch using synthesis method		10
7.	a)	State De- morgan's theorems		2
	b)	Distinguish the following		2+2=4
		a)	Sequential logic and combinational logic	
		b)	Edge triggering and pulse triggering of latch	
	c)	Derive the characteristics equations of j-k flip flop		4
	d)	Use only NAND gate to realize Y=ab +b'c+ca'		3
	e)	Use two half adder and a AND gate to design a full adder		7