Total number of printed pages: 2 **BTech(UG)/3/UECE302**

NOV 2024

DIGITAL SYSTEM DESIGN

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1 a) Draw an RTL inverter circuit and explain its transfer characteristics. Mark the end of saturation and end of cut-off points and evaluate the maximum noise margin for both output states. 6

b) Evaluate FAN OUT of the above circuit assuming R_B=10K, R_C=1K and β=75 and noise margin=0.25V. 6

c) Draw and explain how TTL NAND2 logic circuit with tri-state output work. Specify the state of each transistor in the circuit for all input combinations. Explain how the speed of this logic circuit can be improved. 6+2

2 a) Write a Verilog program to structurally describe a half adder and instantiating it, write a Verilog program to describe a full adder. Explain how test bench helps to verify the function of a Verilog module. 6+4

b) Draw the state diagram of a 4-bit sequence detector which can detect the sequence '0001.' Describe the same as a Moore machine using Verilog HDL. 4+6

3 a) Taking two examples each, differentiate between the postulates and theorems of Boolean algebra. 4

b) What is a Variable Entrant Map (VEM)? Simplify the Boolean function $F(a,b,c,d) = \sum m(1,2,5,6,10,11,12,13)$ using this method. 2+4

c) Design and implement a 4x2 priority encoder which has the following priority at the input i0>i1>i2>i3 and can distinguish all-zero input case. 5

d) Design a 1-bit comparator using basic logic gates. Using two such 1-bit comparators, design a 2-bit comparator. 2+3

PTO

4	a)	Draw and explain the block diagram of an array multiplier which can multiply two 3-bit numbers. Clearly show how many numbers of half adders and full adders are required for this.	4+2
	b)	Implement $F(w,x,y,z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$ using only 2x1 multiplexers.	6
	c)	What are PLDs? Implement $f_1(A,B,C) = \sum m(3,5,7)$ and $f_2(A,B,C) = \sum m(4,5,7)$ using three different types of PLDs.	2+6
5	a)	Discuss any two ways of designing a positive edge-triggered D-flipflop. Describe their working with the help of neat timing diagrams.	8
	b)	What do you understand by the excitation table of a flipflop? Show the design procedure required to convert a D flipflop into a JK flipflop.	2+4
	c)	Design a 4-bit universal register using flip-flops and multiplexers. Explain its operation in various modes detailing the circuit functionality.	6
6	a)	What are the different types of finite state machine (FSM). Design a 3-bit synchronous down counter using T-flipflops.	6
	b)	Draw and explain the working of a 3-bit ripple counter with the help of a timing diagram. Discuss what determines its maximum clock frequency.	4+2
	c)	Using a neat block diagram, explain the basic architecture of an FPGA.	8