Total number of printed pages: 2 **Programme: UG/3rd/UECE302**

DEC 2023

DIGITAL SYSTEM DESIGN

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer any five questions.

1.	a)	Represent $(-59)_{10}$ using 8-bits in sign-magnitude, 1's complement and 2's complement form. Draw and explain the circuit which can implement 2's complement addition.	3+3
	b)	Draw and explain the circuit to perform BCD addition using 4-bit binary adders.	4
	c)	State all the basic postulates of Boolean algebra. Using these, evaluate: (i) $x+1$ (ii) $x+x$ (iii) $\bar{\bar{x}}$ (iv) $x+\bar{x}y$	4+6
2.	a)	List all the single variable boolean functions. Determine the number of distinct boolean functions possible using n-variables.	2+2
	b)	Design a gray to binary code converter circuit using K-map method.	6
	c)	Implement $F(w,x,y,z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$ using only 2x1 multiplexers.	8
3.	a)	Explain the Variable Entered K-map method using the borrow output function of a full subtractor.	6
	b)	Design an 8x3 priority encoder with a 'valid' output. Find the simplified Boolean expression for each output.	6
	c)	Design an array multiplier which can multiply any two 4-bit numbers.	8
4.	a)	Draw and explain the working of a NAND gate based level-triggered D flip-flop. Show how it can be converted into an edge-triggered flip-flop.	6
	b)	Design a 3-bit synchronous counter which will count in forward direction when $x = 0$ and in backward direction when $x = 1$, where x is an external input.	8
	c)	Designs a 4-bit parallel-in parallel-out (PIPO) register based on D flip-flops	6

and explain its operation.

5. a) Design a mode-10 asynchronous (ripple) DOWN-counter and explain its working with the help of timing diagram. 8

   b) Design a Moore-FSM which can detect the sequence 101 with overlap. 6

   c) Design a circuit to generate a pulse that remains HIGH for 3 consecutive clock cycles, goes LOW for the next 2 consecutive clock cycles, and repeats indefinitely. 6

6. a) Implement $f_1(A,B,C) = \sum m(3,5,7)$ and $f_2(A,B,C) = \sum m(4,5,7)$ using appropriate PROM, PAL and PLA architectures. 9

   b) List out and define four most important metrics which determine the performance of any logic families. 4

   c) With the help of a neat circuit diagram, explain the working of a TTL NAND gate. 7

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