Total number of printed pages: 2 **Programme: UG/3rd/UECE302**

2022

DIGITAL SYSTEM DESIGN

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1.	a)	Discuss the steps in converting $(1001.10)_{10}$ into binary and hexadecimal number system up to the place value of 2^{-8}.	5
	b)	Implement $(65)_{10} - (5)_{10}$ and $(5)_{10} - (65)_{10}$ using 2's complement method.	5
	c)	Design a circuit which can convert any 3-bit Grey code to its corresponding binary code.	5
	d)	Implement a single decimal digit BCD adder using 4-bit binary adders and few additional logic gates.	5
2.	a)	Using only the basic postulates of Boolean algebra, prove the following laws. (i) Associative law (ii) De-Morgan's law	6
	b)	Express the Boolean function $f(A, B, C) = \bar{A} + C$ in canonical POS form	6
	c)	Implement a Full Adder using only Half Adder and an additional gate.	4
	d)	Implement a 4X1 MUX using only 2x1 MUXs	4
3.	a)	Write the truth table for common anode 7-segment display decoder.	4
	b)	What is the disadvantage of ripple carry adder? Explain how this is overcome in carry look-ahead adder with the help of neat circuit diagram.	2+6
	c)	Design a priority encoder with 8-bit inputs, 3-bit code output and a single bit valid output.	8
4.	a)	Design and draw the circuit diagram of PROM, PAL and PLA which can implement the following Boolean functions. (i) $f_1(a, b, c) = ab + bc + \bar{a}\bar{b}$ (ii) $f_2(a, b, c) = ab + c$	12

	b)	Design and draw the architecture of a 8K byte ROM which has got a word length of 8 bits. Keep the aspect ratio as minimum as possible.	8
5.	a)	Draw the circuit diagram of a master-slave JK flip flop and explain how it overcomes the race around condition with the help of timing diagram.	5
	b)	Design a digital system to detect a sequence 1001 with overlap using only two flip-flops and an additional combinational circuit.	10
	c)	Implement a universal shift register which can perform (i) store, (ii) left shift, (iii) right shift and (iv) parallel load operations based on external mode selection input.	5
6	a)	Design a mod-10 asynchronous (ripple) up-counter which can count from 4 to 13 and repeat cyclically. Explain its operation using timing diagram.	8
	b)	For a Mode-128 ripple counter, determine the value of maximum propagation delay.	2
	c)	Draw the circuit diagram of a TTL inverter and explain its working and obtain its transfer characteristics showing different regions operations. Explain how this circuit can be modified into a 2-input NAND gate.	8+2

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