Total No. of printed pages = 4

19/3rd Sem/UECE302

2021

DIGITAL SYSTEM DESIGN

Full Marks – 100

Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer any *five* questions.

1. (a) Discuss the procedures to convert a decimal number having integer and fractional part into its binary equivalent. 5

   (b) Show any two ways of representing signed numbers in Binary system. List the range of numbers allocated in each case for n-bit representation. 5

   (c) Distinguish between BCD and Excess-3 codes and list their advantages. 5

   (d) Design a BCD adder using 4-bit binary adder and few additional logic gates. 5

[Turn over

2. (a) State all the basic postulates of Boolean algebra. 4

(b) Using the basic postulates, prove the following for Boolean variables :

(i) $(x')' = x$

(ii) $(a + b) + c = a + (b + c)$. 3+3=6

(c) Write the truth table for all the 2-variable Boolean functions. Give algebraic expression for each case. 3+3=6

(d) With the help of an example, distinguish between prime implicants and essential prime implicants. 4

3. (a) Find the standard POS form of the Boolean function : 5

$F(w, x, y, z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$.

(b) Design a decoder circuit for common anode based 7-segment LED display. 10

(c) Draw the variable entered K-map for the carry output of a full adder and find its simplified Boolean expression. 5

4. (a) Compare the performance of an n-bit ripple carry adder and carry look-ahead adder. Implement a 4-bit carry look-ahead adder using basic gates. 6

(b) Implement $F(a,b,c) = \Sigma(1,2,3,5,6)$ using only 2x1 MUXs. 4

(c) Write the truth table for an 8×3 priority encoder with a 'valid' output. Find the simplified Boolean expression for each output. 6

(d) Implement an SR flipflop using T-flipflop. 4

5. (a) In a serial-in serial-out (SISO) 4-bit right shift register, the complement of the last flipflop, Q0 is given as the input of the first flipflop, D3. Draw the timing diagram. 5

(b) Design a 3-bit synchronous up/down counter using D-flipflop which will count in ascending order when the mode input, M = 0 and down count when M = 1. 10

(c) Draw the Mealy and Moore machine state diagram for a sequence detector which can detect the sequence 0010 with overlap. 5

6. (a) Draw the PROM, PLA and PAL circuits which can implement

$F1(a,b,c) = ab + bc + ac$; $F2(a,b,c) = ab + \bar{b}c$. 10

(b) Draw the circuit diagram of a Universal Shift Register which can store, right shift, left shift and parallel load depending on the value of control input S_1S_0. Write a verilog program to describe the same. 5+5=10

7. (a) Explain the working of RTL based inverter with the help of its circuit and transfer characteristics. 6

(b) With the help of a neat circuit diagram, explain how high impedance output state can be implemented in TTL two-input NAND gate. 6

(c) Explain the Read and Write operation of a 3 transistor DRAM cell using the circuit diagram and necessary waveforms. 8