Total number of printed pages:3

UG/3rd/UECE302

2021

DIGITAL SYSTEM DESIGN

Full Marks: 100

Time: Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. a) Explain the steps involved in converting an M-ary digital signal to its binary equivalent by taking the case of M=100. 4

   b) (i) The binary number corresponding to $(2AC.7E)_{16}$ is _____. 2+2

   (ii) In the binary representation of $(50)_{10}$, the digit in the position corresponding to 2^3 is _____.

   c) Describe a digital controller using pseudocode that can ON/OFF an air cooler if the temperature sensor gives 1°C greater/lesser than the reference temperature. 4

   d) List the basic types of operations available in a Hardware Description Language (HDL). 4

   e) Show how one can synthesize a *for loop* construct in HDL into two very different types of hardware design style. 4

2. a) Write the VHDL code for structural description of a 4x1 multiplexer. 5

   b) What do you understand by a test bench in VHDL? Describe it in the case of a 4x1 multiplexer. 5

   c) In VHDL, distinguish between the following-

(i) 'bit' and 'std_logic' in port declaration 2+3

(ii) Data flow architecture and procedural architecture

d) Describe a 4-bit ripple carry adder in three-level hierarchical architecture. 5

3. a) Explain why we use PMOS transistors to pull-up the output to HIGH voltage and NMOS transistors to pull-down it to LOW voltage. 5

b) Design a CMOS circuit to implement the Boolean function, $Y = \overline{(A + B).C}$ 5

c) Draw the circuit diagram of a TTL inverter and explain its working in different regions of operation as the input voltage is raised from 0 to 5V. 6

d) What are the most important parameters by which we can compare the performance of different logic families? 4

4. a) List out all the Boolean functions possible with the mapping $\{0, 1\}^2 \rightarrow \{0,1\}$ and write the corresponding Boolean expressions. 6

b) Prove the following theorems using the Boolean algebra clearly stating the postulates used in each step. 3+3+3

(i) $x.x = x$

(ii) $x.0 = 0$

(iii) $(x')' = x$

c) Given $f(a, b, c) = a.b + a.c + b.c$, find the canonical POS form using the Boolean algebra and represent it in terms of the maxterms. 5

5. a) Design a 1-bit magnitude comparator with inputs A and B, and outputs G (A >B), L (A<B) and E (A=B). Show 5

that $E = \overline{G + L}$.

b) Distinguish between the operation of common-cathode and common-anode type 7-segment LED display. Write the truth table in each case. 5

c) Find the simplified expression for the Boolean function $f(a, b, c, d, e) = \sum(2,3,6,7,9,13,18,19,22,23,24,25,29)$. 5

d) Explain the principle behind the design of an n-bit look-ahead carry adder and state its advantage over the ripple carry adder. 5

6 a) Implement a 16x1 MUX using only 4x1 MUXs 4

b) Explain how we can implement an 8-variable Boolean function using only 6-variable look up tables (LUTs). 5

c) Design a mod-10 asynchronous counter using negative edge triggered J-K flip-flop having clear inputs. 5

d) Design a Mealy machine which can detect the sequence '110'. 6

7. a) Design the following Boolean functions using PLA and PAL architectures. 4+4

$f_1(a, b, c) = m_0 + m_1$; $f_2(a, b, c) = m_0 + m_2 + m_7$;

$f_3(a, b, c) = m_1 + m_7$;

b) Draw the circuit diagram of a static RAM cell and explain how the write and read operation is conducted. 4

c) What are the disadvantages of purely Finite State Machine (FSM) based digital system design and explain how this is overcome in a Register Transfer Level (RTL) design. Demonstrate it with the help of an appropriate example. 8