Total number of printed pages:4

UG/3rd/UECE301

2021

ELECTRONIC DEVICES

Full Marks: 100

Time: Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1

a. Find the solutions of the Schrodinger's equation for an electron interacting with a potential energy well with infinite boundaries. **10**

b. Compare the direct band-gap semiconductors ~vs~ Indirect band-gap semiconductors with examples. **5**

c. Explain the concept of band splitting due to the interaction of two nearby atoms of same semiconductor material with diagrams. **5**

2

a. Behavior of an electron inside a solid is well explained by quantum mechanical theory i.e. wave-particle duality, Explain the principles/ experiments describing particle and wave nature respectively. **10**

b.Describe the effect of quantum mechanical tunneling for an electron interacting with a potential barrier of finite energy and height.**5**

c. In an intrinsic material the generation rate of free charge carriers is equal to recombination rate at thermal equilibrium. **5**

3

a. Explain the Fermi-Dirac theory in relation to the probability of finding charge carriers in a doped semiconductor material with the help of graphical analysis. **10**

b. Why doping is necessary in semiconductor materials? Describe the types of extrinsic semiconductor with proper examples. **10**

4

a. Starting from the continuity equation, derive the Einstein's relation for semiconductors. You may choose either p-type or n-type semiconductor. **7**

b. The mobility and mean lifetime of a particular type of charge carriers in a semiconductor at room-temperature are $0.36\,m^2/Vs$ and $340\mu s$ respectively. Determine the mean diffusion length. ($k_B = 1.38 \times 10^{-23}\,J/K$). **3**

5

a. Derive the expressions for Hall voltage V_H and Hall coefficient R_H. You may choose either p-type or n-type semiconductor. You should also comment on the significance of Hall effect in semiconductors. **5**

b. The resistivity at room-temperature of intrinsic silicon is $2.3 \times 10^3 \Omega m$ and that of an n-type silicon is $8.33 \times 10^{-2} \Omega m$. A bar of this extrinsic silicon (dimension: $50mm \times 100mm$) has a steady state current of $1\mu A$ and the voltage across the bar is 50 mV. If the same bar is of intrinsic silicon, find the voltage across the bar. **2**

c. The majority carriers in an n-type semiconductor have an average drift-velocity $\vec{v}_d$ in a direction perpendicular to an uniform magnetic field $\vec{B}$. Find the direction of the electric field $\vec{E}$ induced due to Hall effect. **3**

6

a. Starting from the expression for excess carrier concentration across a PN-junction, derive the expression for the diode equation $I = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)\left(e^{\frac{-qV}{k_BT}} - 1\right)$ where the terms have their usual meanings. Your answer must be illustrated by plots of carrier distributions on either side of the depletion region and energy level diagram showing the Fermi level. **6**

b. A one-sided lightly doped junction has 10^{21} dopants per m^3 in the lightly-doped region, zero bias voltage and a built-in potential of $0.2V$. The relative permittivity of the material is 16. Find the depletion width. ($\varepsilon_0 = 8.875 \times 10^{-12}\frac{F}{m}$). **4**

c. In an asymmetrically doped (or abrupt) PN-junction, the doping level on the *n*-side is five times to that on the *p*-side. Find the ratio of the depletion layer width in the *p*-side to the *n*-side. **4**

d. Derive the expression for junction capacitance C_j and discuss its dependence on the type of bias applied (forward and reverse bias). **6**

7

a. Elaborate the working of a *pnp*-BJT with the aid of a diagram (in CB-configuration) showing the current components due to electron and hole flow. From this discussion, derive the relationship between *current transfer ratio* (α) and base-to-collector *current amplification factor* (β). What will happen if the base current is zero? **9**

b. Calculate the I_C, I_E and β for a BJT with $\alpha = 0.99$ and $I_B = 20\mu A$. **3**

c. Discuss the effects of bias-voltage on the base width explaining the Early effect in BJTs with necessary plots and diagrams. **8**

8

a. Explain the ideal C–V characteristics of the MOS capacitor with a sketch of capacitance versus gate voltage. You must discuss the following regions- (i) strong accumulation (ii) weak accumulation (iii) weak inversion and (iv) strong inversion and show them on the plot. 7

b. Derive the expression for drain-current $I_D = G_0 V_P \left[\frac{V_D}{V_P} + \frac{2}{3}\left(\frac{-V_G}{V_P}\right)^{\frac{3}{2}} - \frac{2}{3}\left(\frac{V_D - V_G}{V_P}\right)^{\frac{3}{2}}\right]$ in JFET where the terms have their usual meanings. 8

8c. For an n-channel silicon JFET with half- width of the channel $a = 2 \times 10^{-4}$ cm, resistivity $\rho = 5\Omega cm$ and mobility $\mu_n = 1300\ cm^2/Vs$, determine the pinch-off voltage V_P. Take $\varepsilon_r = 12$ for silicon and $\varepsilon_0 = 9 \times 10^{-14}\ \frac{F}{cm}$. 5