Total number of printed pages = 5

19/6th Sem/UECE 601

2022

DIGITAL VLSI DESIGN

Full Marks – 100

Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer any *five* questions.

1. (a) Explain the pass characteristics of NMOS and PMOS transistors. Which of these is good for pull-up and pull-down network design ? Justify your answer with proper reasoning. 6

   (b) Implement a 2×1 MUX using only transmission gates. Using this as a sub-module, implement the sum output of a full adder. 6

   (c) Draw the basic architecture of an FPGA chip. What are the 3 most important parts of the architecture and explain how it is utilized to implement a logic design. 8

[Turn over

2. (a) Draw the energy band diagram of a MOS structure for the case $\phi_m < \phi_s$ and mark all the energy levels in the diagram. Show how this diagram gets modified when the gate voltage is 8

(i) greater than

(ii) equal to and

(iii) less than the flat band voltage (V_{FB}).

(b) Derive the expression for threshold voltage of an NMOS transistor when

$V_{FB} \neq 0$, $Q_{OX} \neq 0$ and $V_{SB} \neq 0$ 12

3. (a) Design a Moore FSM which can detect both 101 and 010 sequences including overlapping cases. Write a Verilog program to describe the same. 5+5=10

(b) What is Algorithmic State Machine (ASM) ? Taking the example of an Add-Shift multiplier, explain how an ASM chart is utilized to implement the RTL design. 2+8=10

4. (a) Derive the expression for drain current in a PMOS transistor using level-1 SPICE model. 6

(b) Derive the expression for sub-threshold swing in a MOS transistor. Explain how its value determines the ratio between ON current and OFF current. 6

(c) What are the different parasitic capacitances in a MOSFET ? Give mathematical expression for each one of them. Distinguish the design and process parameters in these expressions. 8

5 (a) Draw the static characteristics of a CMOS inverter and mark the different regions of operation of the circuit based on the OFF, triode and saturation modes of the NMOS and PMOS transistors. Mathematically show that, for a CMOS inverter based on long channel devices, $V_{IH} - V_{IL} \cong 2V_{OL}$. 4+6=10

(b) Compute the value of the average channel resistance of an NMOS transistor in a CMOS inverter circuit when the output voltage changes from V_{DD} to $V_{DD}/2$. 5

(c) Distinguish between the different components of power dissipation for a CMOS inverter. Give the expression for each one of them. 5

6. (a) Discuss how interconnects can be modeled as an R-C network. 4

(b) Discuss how the transistor sizing is determined in a 3-input CMOS NAND gate design. Estimate the worst case rising and falling delay of a 3-input NAND driving 'h' identical gates. 4+6=10

(c) Differentiate among the following terms : 6

(i) Parasitic effort

(ii) Logical effort

(iii) Electrical effort in CMOS digital circuits.

7. (a) Design a CMOS circuit to implement the Boolean function $Y = \overline{A + BC + DE}$. Draw the stick diagram for the circuit using Euler's path algorithm. 2+4=6

(b) Draw the layout of a CMOS inverter by orienting the transistors in

(i) vertical direction

(ii) horizontal direction. 3+3=6

(c) Compare the effects of constant field scaling and constant voltage scaling on : 2×4=8

(i) drive current

(ii) intrinsic gate delay

(iii) doping concentration

(iv) power dissipated per unit area.