Total number of printed pages = 8

19/4th Sem/UECE 402

2022

ANALOG CIRCUITS

Full Marks – 100

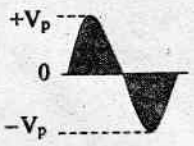
Time – Three hours

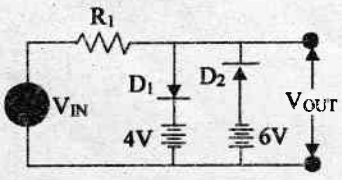
The figures in the margin indicate full marks for the questions.

Answer any *five* questions.

1. (a) Draw the circuit diagram of a full-wave rectifier based on center-tapped transformer and explain its working. Determine the peak reverse voltage across the diode in this circuit. 4+2=6

   (b) Analyze the following circuit and plot its output waveform with proper justification. 4





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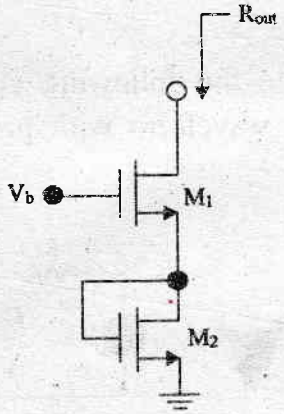
(c) Draw the diagram of a clamper circuit based on Si diode and explain its working with the help of necessary waveforms. 4

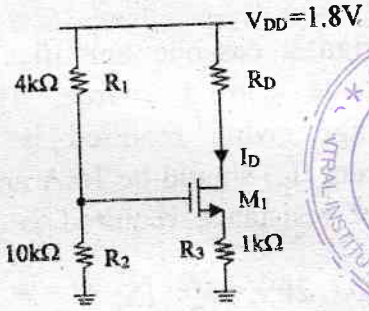
(d) A Si-diode and a 100Ω resistance are connected in series with a 3V DC voltage source. Determine the value of current through the diode using iterative procedure. Given the reverse saturation current as 10^{-15} A. 6

2. (a) Write the expression for drain current of an NMOS transistor in saturation (flat) region of operation. Using Taylor series expansion, find the small signal model for this device assuming it as 3-terminal device. 4

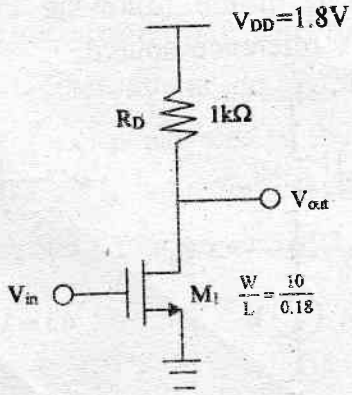
(b) Determine the expression for small signal resistances R_{out} in the circuit given below assuming $\lambda \neq 0$ for both transistors. 4



(c) For the circuit below, $V_{th} = 0.5V$, $k_p = 100\mu = \frac{A}{V^2}$, $\frac{W}{L} = \frac{5}{0.18}$ and $\lambda = 0$. What is the maximum allowable value of R_D for M_1 to remain in saturation? 6



(d) Calculate the small signal voltage gain of the CS stage given below. Given $I_D = 1mA$, $V_{th} = 0.5V$, $k_p = 100\mu\frac{A}{V^2}$ and $\lambda = 0.1V^{-1}$ 6

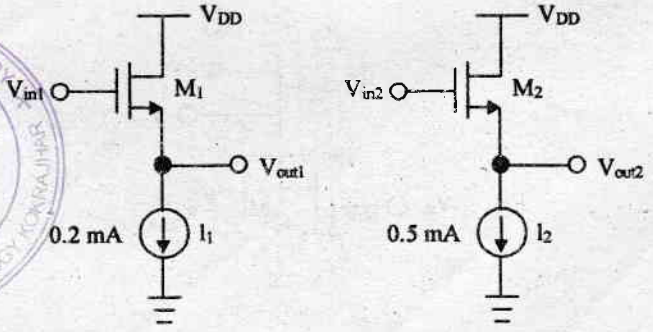


3 (a) Draw the circuit diagram of a Source follower and derive its AC input resistance, output resistance and voltage gain. Explain why it can serve as a good voltage buffer. 5

(b) Derive the necessary small signal parameters of a CG amplifier and model it as current amplifier. 5

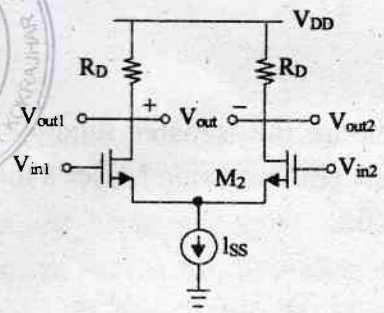
(c) Design a cascode amplifier biased with a cascode current source. The output AC voltage swing required is 12V, the bias current (I_D) should be 1mA and the minimum input resistance required is 500kΩ. Given, VDD = 20V, V_{tn} = 1V, V_{tp} = −1V, $k_p\left(\frac{W}{L}\right)$ =10mA/V², $\lambda = 0.05V^{-1}$. Determine the maximum voltage gain achievable using this configuration. 10

4 (a) Design a current mirror circuit that produces I_1 and I_2 in the following circuits from a 0.3mA reference source. 6



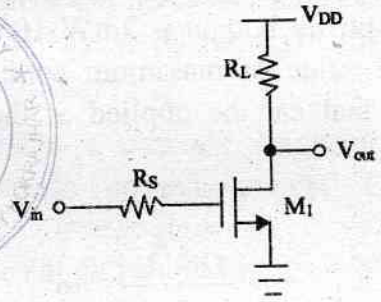
(b) For the MOS differential pair below, if V_{DD}=1.8V, k_p = 100μA/V², λ = 0, find the value of R and (W/L)-ratio of the transistors such that the differential voltage gain is 5, common mode voltage at the output is 1.6V and the power budget is 2mW. If V_{th} = 0.5V, find the value of maximum common mode voltage that can be applied at the input.

6+2=8

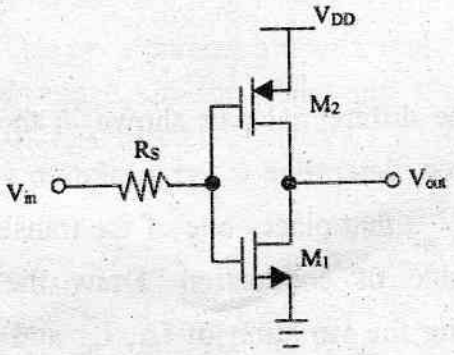


(c) For the differential pair shown in the above question, determine is the minimum value of $|V_{in1}-V_{in2}|$ that places one of the transistors at the edge of conduction. Draw the graph showing the variation of I_{D1}, I_{D2} and V_{out} as a function $V_{in1} - V_{in2}$. 3+3=6

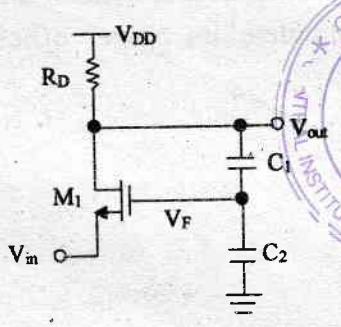
5 (a) Using Miller's theorem, determine the input and output poles of the CS stage depicted below while including the output impedance (r_{ds}) of the transistor. 5



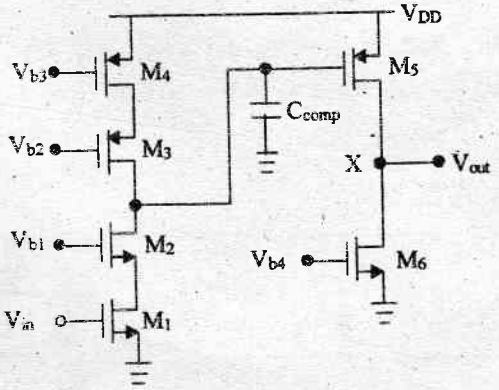
(b) Compute the transfer function of the circuit below without using Miller's theorem. Assume $\lambda = 0$. 10



(c) Consider the feedback circuit shown below where C_1 and C_2 are very small. Compute the closed loop gain, input and output impedance of the circuit. Assume $\lambda = 0$ and neglect all parasitic capacitances. 5



6. (a) The amplifier shown below employs a cascode stage followed by a CS stage. Assuming that the pole at node B is dominant, sketch the frequency response and explain how the circuit can be compensated. 8



(b) Explain the criteria required to build an oscillator using a neat block diagram. 4

(c) Discuss how power efficiency of an amplifier is determined. Draw the circuit diagram of a push-pull amplifier and explain its working. Calculate its power efficiency. 8