Total number of printed pages: **4** **Programme(UG)/4th Semester/UCSE401**

2025

Computer Organization and Architecture

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. a) Find X, Y, Z for $(XYZ)_7 = (323)_8$ 3

   b) What is the largest 5-digit number in base 6 number system? 3

   c) If $(X)_8 + (37)_8 = (106)_8$, find X. 4

   d) Divide $(27)_{10}$ by $(4)_{10}$ using Non-Restoring Division algorithm in binary. 10

2. a) Perform 2's complement subtraction using 8-bit numbers: 8

   i) $\mathbf{(-25)_{10} - (-15)_{10}}$

   ii) $\mathbf{(60)_{10} - (75)_{10}}$

   b) Perform arithmetic right shift on the following 8-bit 2's complement numbers and interpret the result: 2

   10011010 (Shift right by 2)

   c) Find the product of $\mathbf{1011_2}$ and $\mathbf{1101_2}$ using Unsigned Binary Multiplication. 10

3. a) A processor has a 24-bit instruction format with: 10

   Opcode

   One destination register

   One source register

One immediate operand

If the opcode uses 6 bits and the immediate field must be at least 8 bits, how many registers can be supported?

b) A machine has: 10

32-bit instruction length

32 registers

40 distinct instructions

Each instruction has one register operand and two immediate operands (unsigned).

If the first immediate operand uses 10 bits, what is the maximum value of the second immediate operand?

4. a) Consider a 16-bit processor with the following state: 10

Memory Contents:

Address	**Value**
100	600
200	LOAD AC, Mode
201	500
400	700
500	800
600	900
700	1000

Registers:

PC = 200 (Program Counter)

R1 = 300 (Source Register)

Base Register (BR) = 100

The instruction at address 200 is a LOAD into the accumulator (AC), with the Mode field specifying the addressing mode. The value 500 at address

201 may be used in address calculations. Determine the effective address (EA) and the operand loaded into AC for the following addressing modes:

Direct, Immediate, Indirect, PC-relative, Displacement (Base + Offset), Register (R1), Register Indirect (using R1), Autoindexing with increment (using R1)

b) A 5-stage pipeline processor has the following cycle requirements for four instructions (I1, I2, I3, I4) in each stage (S1–S5): 10

	S1	S2	S3	S4	S5
I1	1	2	1	1	1
I2	1	1	3	2	1
I3	2	1	1	1	2
I4	1	2	2	1	1

How many cycles are needed to execute the following loop?

```
for (i = 1 to 3)
{
   I1;
   I2;
   I3;
   I4;
}
```


5. A 32-bit microprocessor is to be interfaced with 1 KB of RAM and 1 KB of ROM. The available memory chips are: 20

RAM chip: 256 × 8

ROM chip: 1K × 8

(a) How many RAM chips and ROM chips are needed to fulfil the memory requirement?
(b) How many address lines are required to access the total memory? Show the diagram.
(c) Suggest a memory map for RAM and ROM (indicate starting and ending addresses in hexadecimal).

6 a) In a computer system 10

(i) How many 32K × 8 RAM chips are needed to provide a memory capacity of 512K bytes?

(ii) How many lines of the address must be used to access 512K bytes? How many of these lines are connected to the address inputs of all chips?

(iii) How many lines must be decoded for the chip select inputs? Specify the size of the decoder.

b) A computer system has the following specifications: 10

Cache: 128 lines (slots), organized as a 4-way set-associative cache

Main Memory: Contains 8K blocks, where each block has 64 words

The word size is 1 word = 4 bytes

(i) How many sets are there in the cache?

(ii) How many bits are required to address a word in main memory?

(iii) Show the format of a main memory address, clearly indicating the number of bits for the Tag, Set Index, and Word Offset.

7 Write short notes on 20

a) Synchronous handshaking

b) Asynchronous handshaking

c) Cache replacement algorithms

d) Working principle of Interrupt Driven I/O