Total number of printed pages: **2** **UG/4th Semester/UCSE401**

2024

Computer Organization and Architecture

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. a) Consider a 4-stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below: 10

	S1	S2	S3	S4
I1	2	2	2	2
I2	1	1	1	1
I3	2	3	3	2
I4	1	1	1	1

What is the number of cycles needed to execute the following loop?

```
for ( i = 1 to 2)
{
        I1;
        I2;
        I3;
        I4;
}
```

b) Explain the working principle of Programmed I/O technique. 10

2. Explain, with examples, four different types of cache replacement algorithms. 20

3. a) A computer uses RAM chips of 1024 * 8 capacity. 10

   i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 16KB?

   ii) How many of these lines will be common to all the chips?

   iii) How many lines must be decoded for the chip select? Specify the size of the decoder.

   b) Describe the key components of a magnetic disk storage system 10

4. a) Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of the main memory is 128 KB. Find the number of bits in the tag field. 10

   b) Show the step-by-step multiplication process using Booth's algorithm when the following numbers are multiplied. 10

   (33) * (-21)

5. What are the different types of addressing modes? Explain with examples. 20

6. Write short notes on 4x5=20

   a) Interrupt driven I/O

   b) DMA

   c) Optical Disk

   d) Demand Paging