Total number of printed pages = 4

19/4th Sem/UCSE 401

RALLIA

#### 2022

## COMPUTER ORGANIZATION AND ARCHITECTURE

#### Full Marks - 100

#### Time - Three hours

The figures in the margin indicate full marks for the questions.

#### Answer any five questions.

- How does the instruction pipeline work? What are the various situations where an instruction pipeline can deviate from its normal operation? What can be its resolutions? 10+5+5=20
- 2. (a) Evaluate the following floating point numbers in decimal form : 5+5=10
  - (i)  $(C1640000)_{16}$  (ii)  $(41200000)_{16}$
  - (b) What are the differences among direct mapping, associative mapping, and setassociative mapping? 10
- 3. (a) Draw a space-time diagram for an eightsegment pipeline showing the time it takes to process ten tasks. 10

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(b) Consider a set associative cache memory with cache size 4K words, block size 64 words and set size 4 blocks. Determine the number of bits in "set" and "word" fields of a main memory address.

4. Write a program to evaluate the arithmetic statement : 20

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- (A \* B) / C D \* (E + F / G) H / (I J \* K)
- (a) Using three address instructions format
- (b) Using two address instructions format
- (c) Using one address instructions format
- (d) Using zero address instructions format.
- 5. (a) Draw the block diagram and label all input and output terminals in the RAM. Explain the function table to specify the operation of the RAM chip.
  - (b) Consider a 16-bit processor in which the following appears in main memory, starting at location 200:

200	Load to AC	Mode	
201	500		
202	Next inatruction		

The first part of the first word indicates that this instruction loads a value into an

73/19/4th Sem/UCSE 401

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accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register ; assume that when used, the source register is R1, which has a value of 600. There is also a base register that contains the value 200. The value of 500 in location 201 may be part of the address calculation. Assume that location 399 contains the value 5000, location 400 contains the value 4999, and so on. Determine the effective address and the operand to be loaded for the following address modes :

FNTRA

- (i) PC relative
- (ii) Displacement
- (iii) Register
- (iv) Register indirect
- (v) Auto increment, using R1
- (vi) Direct
- (vii)Indirect
- (viii)Immediate
- (ix) Auto decrement, using R1.

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(3)

6. Write short notes on :

(a) BUS

(b) Overflow in Arithmetic Operation

(c) r's complement

(d) Memory Hierarchy.

7. (a) What is priority interrupt technique ? Explain parallel priority interrupt technique with the help of a block diagram. 10

# (b) Explain DMA transfer in details with all relevant block diagram. 10



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73/19/4th Sem/UCSE 401

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14.1

20