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53 (IT 303) DLDG

2018

**DIGITAL LOGIC DESIGN**

Paper : IT 303

Full Marks : 100

Time : Three hours

**The figures in the margin indicate full marks for the questions.**

Answer **any five** questions.

1. (i) Write down whether the following statements are *True/False* : 1×10=10
- (a) Hexadecimal 1F converted to binary is 00011100.
  - (b) Karnaugh maps can be used to simplify to boolean function.
  - (c) BCD code of 54 is 101100.
  - (d) The 2's complement of the binary number 1001 is 1110.
  - (e)  $1+1+1 = 10$ .

Contd.

(f) Octal 71 converted to binary is 01110001.

(g)  $1 \oplus 1 \oplus 1 = 1$ .

(h)  $A + AB = A$ .

(i)  $A + B = B + A$  is an example of Commutative Law.

(j)  $1000 - 100 = 0100$ .

(ii) Simplify using boolean algebra :

1×4=4

(a)  $A + A'B$

(b)  $A + AB'C'D$

(c)  $\overline{AB} + AB$

(d)  $\overline{AB} + \overline{AB}$ .

(iii) Simplify the below boolean function  $F$  using Karnaugh map method. 6

$$F(w, x, y, z) = \sum m(0, 1, 3, 5, 6, 8, 9, 10, 11, 12)$$

2. (a) Design a Full Adder. 5

(b) Convert the below function into Canonical form :

$$f(x, y, z) = x' + yz. \quad 3$$

(c) Use only NOR gate to implement Complementary AND, OR functions. 6

(d) Design a 4:1 multiplexer. 6

3. (a) Draw the logic circuit of S-R latch and explain its function with truth table. 2+4=6

(b) Explain the truth table of 2-K latch along with its logic diagram. 5

(c) Write few important differences between Sequential and Combinational circuits. 3

(d) Use basic gates only to implement the below boolean function. 4

$$Y = f(a, b, c) = ab'c + (a' + b)(c' + d')$$

(e) Use only NAND gate to implement  $Y = AB$ . 2

4. (a) Describe the operation of a Master Slave DFF with block diagram. 6

(b) Simplify the below function using K-map method : 6

$$f(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 7, 8, 9, 11) + d(6, 12)$$

- (c) Draw the block diagram of a 3-bit ripple carry adder. 2
- (d) Write down the truth table of a 1:4 de-multiplexer. 2
- (e) Describe the operation of a 2-bit register. 4
5. (a) Convert the following :  $1 \times 8 = 8$
- (i)  $(F1F)_{16} = (-)_2$
- (ii)  $(A1A)_{16} = (-)_2$
- (iii)  $(1001)_2 = (-)_{10}$
- (iv)  $(F1)_{16} = (-)_{10}$
- (v)  $(23)_{10} = (-)_2$
- (vi)  $(42)_8 = (-)_{10}$
- (vii)  $(24)_8 = (-)_2$
- (viii)  $(A1)_{16} = (-)_{10}$
- (b) State and prove De Morgan's law. 6
- (c) Explain the operation of a 1-bit comparator. 4
- (d) Draw the block diagram of a 8:1 Multiplexer. 2

6. (a) Explain the operation of a 2-bit asynchronous counter with block diagram, timing diagram. 12
- (b) Explain the operation of a 2 to 4 Decoder. 6
- (c) Draw the block diagram of a 16:1 Multiplexer. 2
7. (a) Design a Mod-5 counter using J-K flip-flop. 12
- (b) Distinguish between : 2×3
- (a) Excitation table and Truth table
- (b) Encoder and Decoder
- (c) Multiplexer and Demultiplexer.
- (c) Use 2's complement method to subtract 1001 - 0101. 2

10) Explain the operation of a 2-bit asynchronous counter with block diagram using D flip-flop.

11) Explain the operation of a 2 to 4 decoder.

12) Draw the block diagram of a 2 to 4 decoder.

13) Design a Mod-2 counter using JK flip-flop.

14) Distinguish between:

(a) Latches and flip-flops and their uses.

(b) Encoder and Decoder.

(c) Multiplexers and Demultiplexers.

15) Use the Karnaugh map method to simplify the following expression.