53 (IT 303) DLDG

2017

DIGITAL LOGIC DESIGN

Paper : IT 303

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Convert the following : 6

   (i) $(110{\cdot}1)_2 = (?)_{10}$

   (ii) $(FOF)_{16} = (?)_2$

   (iii) $(1F{\cdot}1)_{16} = (?)_{10}$

   (iv) $(49{\cdot}125)_{10} = (?)_2$

   (v) $(21{\cdot}7)_8 = (?)_2$

   (vi) $(10000{\cdot}0010)_2 = (?)_8$

(b) Use Boolean algebra to simplify the following Boolean equation.

(i) $f(x, y, z) = (x + \bar{x}y)\,\bar{x} + \overline{xy\bar{z}}$ 2

(ii) $f(A, B, C) = (A + AB)\,A + A + A'BC$ 2

(iii) $f(a, b, c) = \overline{(a + bc)(a + bc')}\,\{(a'b'c')' + a'\}$ 2

(iv) $f(x, y, z) = xyz + x'y'z + xy'z' + x'y'z' + x'yz$ 3

(c) Prove that : 5

(i) $\overline{a + b + c} = \bar{a}\,\bar{b}\,\bar{c}$

(ii) $\overline{ab} = \bar{a} + \bar{b}$

2. (a) 1×5=5

(i) 2's complement of 101110 is _____.

(ii) $1 \oplus 1 \oplus 0 \oplus 1 =$ _____.

(iii) Excess-3 code of 121 is _____.

(iv) BCD code of 149 is _____.

(v) 0 + 1 + 1 + 1 = _____.

(b) Find out the logic circuit using basic gates.

$Y = f(x, y, z) = \overline{x}(\overline{x} + \overline{y})\,\overline{xy} + \overline{xyz}$

without simplifying the Boolean function above. 3

(c) Use NOR gate only to implement

$Y = x + y + z$ 2

(d) Subtract 10111 – 10000 using 2's complement method. 2

(e) Design a Full subtractor. 8

3. (a) Define with example : 2+2=4

(i) Minterm

(ii) Maxterm.

(b) Simplify using *k*-map method. 4×2=8

(i) $\sum m(0, 1, 2, 4, 9, 11, 13, 14, 15)$

(ii) $f(A, B, C, D) = \sum m(1, 2, 9, 14) + d(0, 3, 11, 12)$

(c) Design a 8 : 1 Multiplexer. 8

4. *(a)* Explain the operation of a J-K latch with truth table and circuit diagram. 5

(b) Draw the circuit diagram of a 2 bit ripple carry adder. 2

(c) Draw the block diagram of a 3 bit asynchronous counter. 2

(d) Distinguish between : 2×3=6

(i) synchronous and asynchronous circuit

(ii) combinational and sequential circuit

(iii) truth table and state transition table.

(e) Explain the operation of a Master-Slave D-Flip Flop. 5

5. *(a)* Design a Mod-5 counter using J-K flip flop. 13

(b) Explain the 2 bit synchronous counter with timing diagram. 7

6. *(a)* Design a 2 bit Magnitude comparator. 7

(b) Write down the truth of a 7 segment decoder. 4

(c) What is race around condition? 2

(d) Draw the circuit diagram of a T-latch. 2

(e) Write down the truth table of a BCD adder. 5

7. (a) Design a Mod-7 synchronous counter using D-Flip Flop. 14

(b) Design a 1 : 8 De-Multiplexer. 6