53 (IT 301) COAR

2019

COAR

Paper : IT 301

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* A microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching and initial decoding of the instruction takes 10 clock cycles. Thereafter, it takes 15 clock cycles to transfer each byte. The microprocessor is clocked at a rate of 10 *GHz.* 10

Contd.

(i) Determine the length of the instruction cycle for the case of a string of 64 bytes.

(ii) What is the worst case delay for acknowledging an interrupt if the instruction is non-interruptible ?

(iii) Repeat part *(ii)* assuming the instruction can be interrupted at the beginning of each byte transfer.

(b) Draw the block diagrams of RAM and ROM chip and explain. 10

2. *(a)* Convert $-153{\cdot}81\times10^{-5}$ into 32-bit IEEE 754 floating point format. 10

(b) Consider a 16-bit processor in which the following appears in main memory, starting at location 200 : 10

200	Load to AC	Mode
201	500	
202	Next instruction	

The Mode field specifies an addressing mode and, if appropriate, indicates a source register ; assume that when used, the source register is R1, which

has a value of 400. There is also a base register that contains the value 100. The value of 500 in location 201 may be part of the address calculation. Assume that location 399 contains the value 999, location 400 contains the value 1000, and so on. Determine the effective address and the operand to be loaded for the following address modes :

Direct, Immediate, Indirect, PC relative, Displacement, Register, Register indirect, Autoindexing with increment, using R1.

3. *(a)* List and briefly explain various ways in which an instruction pipeline can deal with conditional branch instructions. 10

(b) Perform the following arithmetic operations with the decimal numbers using signed 10's complement representation for negative numbers : 10

(i) $(-638)+(+785)$

(ii) $(-638)-(+185)$

4. *(a)* What are the differences among direct mapping, associative mapping, and set-associative mapping? 10

(b) Convert the following: 10

(i) $(12121)_3$ to binary number

(ii) $(4310)_5$ to decimal number

(iii) $(198)_{12}$ to octal number.

5. Write a program to evaluate the following arithmetic statement: 20

$$\chi = \frac{A-(B+(C-D)*E)*F}{G*H-K}$$

(i) using a general register computer with three address instructions

(ii) using a general register computer with two address instructions

(iii) using an accumulator type register computer with one address instruction

(iv) using a stack organized computer with zero address instruction.

6. Given the following specifications for an external cache memory: four-way set associative; line size of two 16-bit words; able to accommodate a total of 4K 32-bit words from main memory; used with a 16-bit processor that issues 24-bit addresses. Design the cache structure with all pertinent information and show how it interprets the processor's addresses. 20