53 (IT 301) COAR

2018

COMPUTER ORGANIZATION AND ARCHITECTURE

Paper : IT 301 (Back)

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* What is the decimal equivalent of the 32-bit IEEE floating point value CC4C0000 ? 10

   (b) What are the different ways of representing signed values ? Give examples. 10

2. *(a)* What is the difference between a direct and an indirect address instruction ? How many references to memory are needed for each type of instruction to bring an operand into a processor register ? 4

(b) Write a program to evaluate the arithmetic statement

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

(i) using a general register computer with three address instructions

(ii) using a general register computer with two address instructions

(iii) using an accumulator type register computer with one address instruction

(iv) using a stack organized computer with zero address instruction.

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3. (a) Convert the following decimal numbers into binary and hexadecimal forms :

(i) 25·5 (ii) 25555 10

(b) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the efffective address if the addressing mode of the instruction is

(i) direct (ii) immediate (iii) relative

(iv) register indirect

(v) index with R1 as index register.

10

4. *(a)* Convert 1234.125 into 32-bit IEEE floating point format. 10

(b) Show the step-by-step multiplication process using Booth's algorithm when the following numbers are multiplied.

$$(15)\times(-13)$$ 10

5. *(a)* Determine the number of clock cycles that it takes to process 200 tasks in a six segment pipeline. 6

(b) A non-pipeline system takes 50 *ns* to process a task. The same task can be processed in six-segment pipeline with a clock cycle of 10 *ns*. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved ? 14

6. An 8-bit computer has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32*K* bytes of memory. The high order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32*K* bytes each, for a total of 256*K* bytes of memory. 20
