53 (IE 712) CPCN

2019

COMPUTER PROCESS OF CONTROL

Paper : IE 712 (Backlog)

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Draw the block diagram of a digital control system and explain the functions of different components. 10

   (b) Draw and analyze the loop structure with continuous Process and digital controller. 10

2. *(a)* What are the different algorithms used for implementation of analog controllers? Derive the algorithms for PI Controller using backward rectangular rule for integration term. 10

(b) Derive the differences betweet equation of $u(k)$ vs. $e(k)$ for PID Control using trapezoidal rule for integration term. Find the change in output at third sample for the following data: $k_p = 2, T = 0.2\,sec$, reset time = 2 sec^{-1}, derivative time = 5 *sec*, $e_1 = 2$, $e_2 = 1$ and $e_3 = 3$. 10

3. *(a)* State and prove the Final Value Theorem (FVT) for *z*-transformation. Find the Final value *f(k)* using FVT for a given function:

$$f(z) = \frac{2.508z^2}{(z-1)(z^2+0.165z+0.616)}$$ 10

(b) Using the *z*-transformation find $x(z)$ when $x(k) = \left(\frac{1}{7}\right)^k$ for $k = 0,1,2,3....$ 5

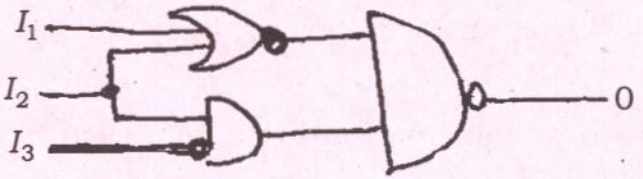
(c) Find the closed loop solution of the following difference equation:

$$x(k+2)+3x(k+1)+2x(k)=0$$

Given $x(0)=0$ and $x(1)=1$. 5

4. *(a)* Draw the block diagram of PLC and explain the function of each block. 5

(b) Convert the following logic gate to PLC ladder diagram (I-input, O-output). 5



(c) Explain the operation of PLC timer with a suitable example. 10

5. *(a)* Draw the block diagram of a Distributed Control System (DCS) and explain the functions of different components. 10

(b) Explain, with a schematic diagram, the operation of direct digital control system. 10

6. *(a)* Derive the generalized equation of a controller for a digital control system. Using this equation, derive a deadbeat controller algorithm. 10

(b) The open loop transfer function of a process is given by $G(s)\frac{e^{-2s}}{10s+1}$. Design a deadbeat digital controller for the system to achieve a closed loop time constant of 5 sec. Assume that the sampling time, T=1 *sec.* 10

7. Write short notes on ***any two*** of the following : 20

(a) Stability of discrete data system

(b) Pole-Zero method for signal discretization

(c) Jury's Stability test

(d) Realization of full adder using PLC ladder diagram

(e) SCADA.