53 (IE 501) MPMC

2017

MICROPROCESSOR AND MICROCONTROLLERS

Paper : IE 501

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Define the terms word and instruction for any microprocessor based system. 2

(b) Mention *two* differences between : 2+2=4

(i) Compiler and interpreter

(ii) Machine language and Assembly language.

(c) What is the function of Flag register in 8085 ? How are zero(z) and carry (cy) flags affected ? 1+2=3

(d) Specify the Byte size and meaning of the following instructions — 5×1=5

(i) MOV B,M

(ii) LDA 2005 H

(iii) CMA

(iv) SHLD A000H

(v) CPI 03 H

(e) Design a flowchart and write a program in Assembly language to add two 8-bit data and display the SUM and CARRY at parts 01 H and 02 H respectively. 6

2. (a) What are the internal data operations performed by 8085 *μp* ? Explain with an example. 5

(b) Explain how flip-flops can be used to construct an *n*-bit register with the help of diagram. 5

(c) If the size of a memory chip is 1024 × 4 bits, how many such chips will be required to make up a 4*k byte* memory system ? 2

(d) Briefly explain each of the Control and Status signals present in 8085 μp. 5

(e) Define the terms — T-state, Machine cycle and Instruction cycle. 3

3. (a) The last memory location of a (4096×8) EPROM is FFFFH. Find its starting address and design a system for this EPROM to be interfaced with 8085 μp with the help of a 3×8 decoder. 2+6=8

(b) Explain the instruction STA D050H with the help of its bus timing diagram. 6

(c) Find the member of M-cycles and T-slates and time required to execute the following instructions if the system has a clock frequency of 2*MHz*. *(i)* MOV A,M *(ii)* JMP 2000H *(iii)* MVI A, 05H. 3×2=6

4. (a) Can an input port and an output port have the same port address ? Justify your answer. 2

(b) Mention at least *six* differences between Peripheral I/O and memory-mapped I/O technique. 3

(c) Write an Assembly language program to add all the data which are less than OAH present in memory locations starting at D000 H to D008 H. The total sum and carry should be saved for future use. 6

(d) Specify the register contents and status of carry and zero flags after the execution of following instructions — 3×3=9

(i)
```
MVI A, 06H
MVI B, FOH
ADD B
XRA A
```

(ii)
```
MVI A, FFH
ADD A
DCR A
```

(iii)
```
MVI A, FEH
MVI B, 03H
ADD B
ORA A
```

5. *(a)* Explain the meaning of following instructions with suitable examples.

3×3=9

(i) RAL

(ii) CALL I000H

(iii) PUSH D

(b) Specify the number of times the following loops are executed —

3×2=6

(i)

```
        MVI A, 12H
LOOP :  DCR A
        JNZ LOOP
```

(ii)

```
        MVI A, DAH
LOOP :  RLC
        JC LOOP
```

(iii)

```
        MVI A, 00H
LOOP :  DCR A
        JC LOOP
```

(c) Find the total time delay required to execute the following instructions — (clock frequency = *2MHz*) 2+3=5

(i)

```
        MVI B, 10 H
LOOP 2 : MVI C, FF H
LOOP 1 : DCR C
         JNZ LOOP 1
         DCR B
         JNZ LOOP 2
```

(ii)

```
        L×I B, FFFF H
LOOP : DCX B
       MOV A, C
       ORA B
       JNZ LOOP
```

6. (a) With the help of PUSH and POP instructions, write a program to find out the status of cy and z flags by displaying at port 02 H. 5

(b) Answer the following questions briefly— 4×2=8

(i) Is there a minimum pulse width required for INTR signal ?

(ii) If more than one interrupt requests are activated simultaneously, how does 8085 μp handle it ?

(iii) Specify the CALL locations for vectored interrupts of 8085 μp.

(iv) State the functions of instructions EI and DI.

(c) The Hex code of RST 7 instruction is FFH. Explain the meaning of this instruction and design a circuit to implement this instruction with the help of tri-state buffer. 7

7. (a) List the basic requirements for a programmable interfacing device and briefly explain each of their functions. 6

(b) Draw the block diagram of 8155 multipurpose programmable device and explain the function of each block. 10

(c) How many lines are present in the control logic of 8255A programmable peripheral interface ? State the function of each line. 4