Total No. of printed pages = 6

RETEST EXAMINATION - 2019

Semester : 5th

Subject Code : Et-502

MICROPROCESSOR

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

Instructions :

1. *All* questions of PART – A are compulsory.
2. Answer any *five* questions from PART – B.

PART – A

Marks – 25

1. Fill in the blanks : 1×10=10

   (a) In 8085 MP, carry flag is ——— when an arithmetic operation results in carry.

   (b) ——— bus is bidirectional.

   (c) In 8085 read and write control signals are active.

[Turn over

(d) The ——— signal is used in DMA data transfer.

(e) There are ——— numbers of instructions in 8085.

(f) To select the register of 2K ROM ——— numbers Of address lines are required.

(g) The numbers Of lines in a memory page are ———.

(h) The ——— is a logic circuit that amplifies the current or power.

(i) INTR is an ——— initiated signal.

(j) SRAM is ——— than DRAM.

2. Write true or false : 1×10=10

(a) The address space size of 8085 is 16 bit.

(b) There are 8 numbers Of interrupts in 8085.

(c) MVI M, 8 bit is an example of direct addressing.

(d) In 8085 total numbers Of pins for address bus and data bus are 24 numbers.

(e) The memory address of the last location of 8K byte memory chip is FFFF H. The starting address is E000H.

(f) The fetch cycle has 2 machine cycles.

(g) Intel 8251 is used for serial data transmission.

(h) When CALL is executed, the stack pointer register is decremented by one.

(i) TRAP is a maskable interrupts.

(j) In 8085, control bus consist of 8 numbers Of lines.

3. Choose the correct answer : 1×5=5

(a) In 8085 the pins for +5 input and ground are

(i) 20 and 40 respectively

(ii) 40 and 20 respectively

(iii) 1 and 2 respectively

(iv) None of the above

(b) The numbers Of machine cycles required to execute the instruction STA 2050 H are

(i) 1 (ii) 2

(iii) 3 (iv) 4

(c) In 8085, which instructions are useful for using and writing subroutines ?

(i) PUSH and POP

(ii) CALL and RET

(iii) JMP and RET

(iv) None of the above

(d) If the memory chip size is 1024×4 bits, the chips required to make 2K byte of memory are

(i) 2 (ii) 3

(iii) 4 (iv) 8

(e) ALE stands for

(i) Address latch enable

(ii) Accumulator latch enter

(iii) Address latch enter

(iv) Accumulator latch enable.

PART – B

Marks – 45

4. (a) Draw the block diagram of DMA controller and explain the working in brief. 7

(b) What is master and slave mode in DMA ? 2

5. (a) Draw the block diagram of 8255 and explain it briefly. 6

(b) Draw the control word format of 8255 of I/O mode. 3

6. (a) What is timing diagram ? 2

(b) Draw the timing diagram for IN 01H and explain. 7

7. (a) Classify different types of instructions and give example of each. 3

(b) Write an assembly languge program to find 2's complement of a 16 bit number and store the result in memory locations. 6

8. (a) What are high level languages ? 2

(b) Write an ALP to find largest number in an number array. 7

map for 2K RAM whose starting address is 9800H. Specify the address of the last location on the chip and the number of pages in the chip. 6

(b) Explain the significance of the don't care address lines on memory address of a memory map. 3

10. (a) What is serial bus standard ? Write about the RS 232C bus standard. 1+3=4

(b) Write briefly about the interfacing of μp with Stepper motor with neat diagram. 5

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