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END SEMESTER EXAMINATION - 2019

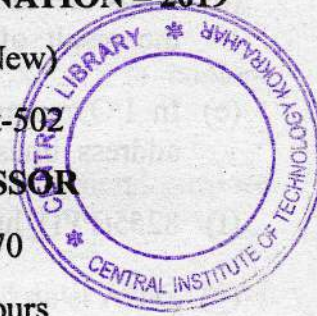
Semester : 5th (New)

Subject Code : Et-502

MICROPROCESSOR

Full Marks - 70

Time - Three hours



The figures in the margin indicate full marks for the questions.

Instructions :

1. *All* questions of PART - A are compulsory.
2. Answer any *five* questions from PART - B.

PART - A

Marks - 25

1. Fill in the blanks : 1×10=10
 - (a) One machine cycle consists of _____ to six T-states.
 - (b) ALE is _____ at the beginning of the operation.

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- (c) In 8085 read and write control signals are active _____.
- (d) Flags are used to _____ the conditions of the result of an operation.
- (e) In I/O mapped I/O, the MPU uses _____ address lines to identify I/O devices.
- (f) 8255(PPI) has _____ I/O pins.
- (g) DMA is an I/O technique commonly used for _____ speed data transfer.
- (h) The level of the pin _____ decides the operating modes of 8086.
- (i) Memory address capacity of 8086 is _____.
- (j) The numbers of data lines in 8086 are _____.
2. Write true or false : $1 \times 10 = 10$
- (a) In 8086 the term HMOS is high speed data transfer.
- (b) INTR has the highest priority among the interrupts in 8085.
- (c) The sign flag is set when the contents of accumulator become negative during an operation.

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- (d) Port B of 8255 can be used as two port.
- (e) CMP means complements the content of the accumulator.
- (f) The meaning of ADD CX, AX is content of AX will be added with CX.
- (g) In 8086 there are four 8-bit general purpose register.
- (h) PUSH and POP are used to enter and retrieve the data to and from the stack.
- (i) In 8259 IRR has eight input lines for interrupt.
- (j) In 8085 JMP 16 bit address is an conditional branching instruction.
3. Choose the correct answer : $1 \times 5 = 5$
- (a) The numbers of interrupt lines in 8085 is
- | | |
|---------|--------|
| (i) 2 | (ii) 3 |
| (iii) 4 | (iv) 5 |
- (b) The number/numbers of machine cycles required to execute the instruction STA 2050H is/are
- | | |
|---------|--------|
| (i) 1 | (ii) 2 |
| (iii) 3 | (iv) 4 |

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(c) DMA controller 8257 has the channels

- (i) 2 (iii) 3
- (ii) 4 (iv) 6

(d) Stack segment is a 16 bit register containing address of

- (i) 1Mb (ii) 64 KB
- (iii) 256 Kb (iv) 2Mb

(e) The 8086 is a microprocessor of

- (i) 8-bits (ii) 16-bits
- (iii) 64-bits (iv) 32-bits

PART - B

Marks - 45

4. (a) What is high level language? Give example. What is mnemonics? 1+2=3

(b) Why RAM is called random access memory? Write about the SRAM and DRAM briefly. 1+5=6

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5. (a) What is timing diagram? If operating frequency is 3 MHz, what will be the time required to execute opcode fetch cycle? 2+1=3

(b) Draw the timing diagram for STA 8050H and explain. 6

6. (a) Why BUS is required in 8085 MP and why data bus is bidirectional? 2+1=3

(b) Explain with the help of proper diagram, the memory read operation. 6

7. (a) What are the different segment registers and what are the advantages of segmentation? 1+3=4

(b) In 8086 what are the different classes of instructions? Explain two of them with examples. 5

8. (a) Explain demultiplexing of AD₀ to AD₇ with proper diagram. 5

(b) What is subroutines and counter in 8085 programming? 4

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9. (a) Write an ALP to find 2s complement of a 16-bits number. 6
- (b) Write an ALP to find larger number of two 8-bits. 3
10. (a) Why 8255 is required in 8085 MPU ? Describe mode 1 of 8255. 2+3=5
- (b) Describe the control word format of 8255. 4
11. (a) What task are done by 8259 (PIC)? 2
- (b) Draw the internal block diagram of 8259 and explain. 7

