END SEMESTER EXAMINATION - 2019

Semester: 4th

Subject Code: Et - 403

DIGITAL ELECTRONICS

Full Marks - 70

Time - Three hours

The figures in the margin indicate full marks for the questions.

Instructions:

- 1. All questions of PART A are compulsory.
- 2. Answer any five questions from PART B.

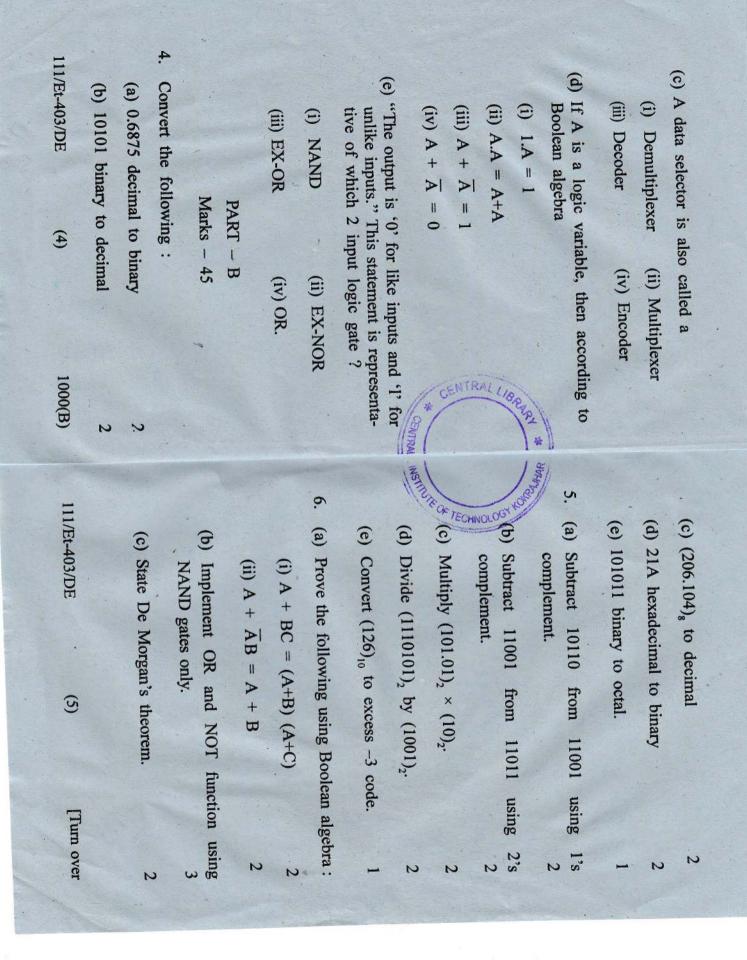
PART - A

Marks - 25

- 1. Fill in the blanks with suitable words: $1 \times 10=10$
 - (a) $(3AC)_{H} = (----)_{2}$.
 - (b) A + BC = (A+B) (-).
 - (c) The result of EX-OR of two equal binary numbers is ———.

[Turn over

1/Et-403/DE (2)		(d) A NOR gate is equivalent to bubbled AND	(c) Another name for digital circuits is logic circuits.	(b) A logic circuit with four inputs can have 8 possible input combinations.	(a) An encoder converts decimal numbers to binary and other codes.		(j) The flip-flop is the fundamental block of lip-flop is the flop is the fundamental block of lip-flop is the flop is the fl	to a universal gate.	memory.	(g) A digital counter is used to count ———.	(1) The outputs of a billary adder are SUM and	(e) A flip-flop can store a ——— bit.	(d) A single input NAND gate is equivalent to a ——— gate.
111/Et-403/DE	(iii) 8	(i) 4	(b) The maximum be used in the	(iii) 10	(i) 4) Minimum construct	MSTIDES 3. Spec	values are	TOOK (I)		(g) J-K flip-flop i	(f) A latch is c coupled AND	(e) In signed bina bit.
(3) [Tum over	(iv) 10	(ii) 6	The maximum number of variables that can be used in the minimization of K-map.	(iv) 5	(ii) 3	number of flip-flops needed to a BCD decade counter is	answer: 1×5=5	ladder DAC four input resistor required.	Each combination of the variables in a truth table is called Minterm.	A Full adder can be implemented with half adders and NOT gate.	J-K flip-flop is called universal flip-flop.	A latch is constructed using two cross-coupled AND or NOR gates.	binary numbers MSB is the sign



7. Define a decoder. Draw a BCD to decimal decoder. Show how to convert the system into demultiplexer. Name two demultiplexer IC's.

1+4+2+2=9

- 8. (a) Draw a 4 bit serial-in-serial-out shift register.

 Draw the waveform of the shift register for serial input data 1011.

 3+3=6
 - (b) Differentiate between static and dynamic RAM.
- 9. (a) Draw the logic diagram of 3 bit simultaneous analog to digital converter and explain briefly the operation. 2+3=5
 - (b) Compare MOS circuit with TTL circuit. 4
- 10. Write short notes on any three: $3\times 3=9$
 - (a) 8:1 multiplexer
 - (b) Master slave JK flip-flop
 - (c) Parity checker/generator
 - (d) Hard disk.

