Total number of printed pages–4

53 (EC 602) VLSI

2021

VLSI DESIGN

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions out of **seven**.*

1. *(a)* Explain what do you understand by 'fabrication yield'. 5

   (b) Discuss the differences between photolithography and e-beam lithography. 5

   (c) List the advantages of ion-implantation technique over thermal diffusion for doping the semiconductor material. 5

Contd.

(d) Compare thermal oxidation of Silicon material using

(i) pure oxygen and

(ii) steam. 5

2. (a) What are the steps involved in creating a p-MOS transistor on a p-type Si-substrate ? Briefly explain each step with the help of neat diagrams. 10

(b) Draw the layout of a CMOS 2-input NAND gate. Explain how $\left(W/L\right)$ ratio of n-MOS and p-MOS are decided for optimum performance of the gate. 10

3. (a) Explain the pass characteristics of an n-MOS and p-MOS transistor. Explain how transmission gate based on CMOS takes the advantages of both transistors. Draw the circuit diagram of a 2×1 MUX using CMOS transmission gates. 10

(b) Give the definition for threshold voltage of an n-MOS and p-MOS transistor. Derive the expression for threshold voltage of an n-MOS transistor using the concept of surface potential. 10

4. *(a)* Derive the level–I Spice model drain current equation for an n-MOS transistor. What is channel length modulation and explain how it will affect the drain current? 10

(b) Draw the transfer characteristics of a CMOS inverter. Discuss how $\left(W/L\right)$ ratio of each transistor influence the transfer characteristics ? Find the expression for static power loss in a CMOS inverter. 10

5. *(a)* Explain how various performance factors change when a MOS transistor is scaled by maintaining—

(i) constant voltage, and

(ii) constant field. 10

(b) Discuss the different parasitic capacitances in a MOSFET. Explain how they influence the dynamic characteristics of an inverter. Estimate the value of propagation delay of a CMOS inverter. 10

6. *(a)* Write a VHDL/Verilog program for describing the following digital circuits—

(i) 4×1 MUX

(ii) 4-bit binary adder. 10

(b) Describe the architecture of a 4-bit ALU which can perform at least 8 different operations depending upon the control signal inputs. 10

7. (a) Draw the circuit diagram of an SRAM cell and explain the READ and WRITE operation with the help of necessary waveforms. 8

(b) What is an FPGA? Describe its architecture with the help of a neat diagram and briefly explain the function of each part. 6

(c) Design a PAL circuit which can implement a full subtractor and a full adder. 6