Total number of printed pages–4

53 (EC 602) VLSI

2019

VLSI DESIGN

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Discuss the sequence of processes/ steps involved in the making of an Application Specific Integrated Circuit (ASIC). Give a brief description of each step involved. 10

   (b) What do you understand by FPGA ? Explain how it differs from ASIC. 5

   (c) Write a verilog program for the design of a full subtractor circuit using basic logic gates. 5

Contd.

2. *(a)* Draw the architecture of a 4-bit ALU and discuss all the operations that can be realized on two 4-bit binary numbers using 3-control inputs and 1-carry input. 10

(b) Design 4×4 array multiplier using full adders and half adders. Discuss the maximum delay involved in evaluation of the final result. 10

3. *(a)* Realize the following boolean functions using PLA and PAL— 10

$f_1(A, B, C) = \overline{A}B + AC$

$f_2(A, B, C) = \overline{A}\,\overline{B} + \overline{B}C$

$f_3(A, B, C) = \overline{A}B + \overline{A}C + A\overline{B}C$

(b) Distinguish between the design of 1T DRAM and 3T DRAM. Explain the read and write operations with necessary waveforms. 10

4. *(a)* Design a CMOS circuit which can implement $Y(A, B, C, D) = (AB + \overline{A}\,\overline{C})D$ and draw its surface layout. 10

(b) Draw a BiCMOS circuit which can implement XOR gate with minimum propagation delay. Explain its working and discuss its disadvantages. 10

5. *(a)* Draw and explain the voltage transfer characteristics (VTC) of a CMOS inverter. Evaluate the expression for midpoint voltage and discuss the effects of increasing $\left(\frac{W}{N}\right)_n$ relative to $\left(\frac{W}{N}\right)_p$ on the VTC curve. 10

(b) Derive the formula for static and dynamic power dissipation in a CMOS inverter. 6

(c) Discuss how the rise and fall times of a CMOS circuit changes with the change in load capacitance. 4

6. *(a)* Discuss how constant field scaling of MOS devices affect the current level and power dissipation in a device. 5

(b) What are the different parasitic capacitances that are included in the switching model of a MOSFET ? Give expressions for each one of them. 5

(c) Draw the energy band diagram for a MOS device with negative flat-band voltage. Derive the expression for threshold voltage using full depletion approximation. 10

7. *(a)* Discuss *any five* DRC rules for mask design using appropriate diagrams. 5

(b) What are the process steps required for fabricating a p-MOS device on a p-substrate? Explain each step using appropriate diagrams. 10

(c) Write a short note on ion-implantation. Give an approximate expression for ion-distribution after the process. 5