53 (EC 602) VLSI

2019

VLSI

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer ***any five*** *questions.*

1. *(a)* Discuss the processing steps involved in fabricating an nMOSFET device with polysilicon gate on a lightly doped *p*-type wafer. 10

   (b) Explain the Ion implantation and Diffusion processes, and discuss their individual advantages and disadvantages. 10

2. *(a)* Discuss how the energy band diagram of an MOS device varies with the magnitude of gate voltage. Derive the expression for threshold voltage of an nMOS transistor. 10

(b) Derive the expression for drain current for an enhancement type nMOSFET in the gradual channel approximation. Evaluate the value of linearized drain-source resistance for the same device if $W = 8\mu m$, $L = 0{\cdot}5\mu m$, $k_n' = 180\,\mu A/V^2$, $V_{T_n} = 0{\cdot}7V$ and $V_{DD} = 3{\cdot}3V$. 10

3. *(a)* Implement the boolean function $f = \overline{AB + C}$ using CMOS logic and draw its corresponding layout. 10

(b) Draw a switching model for a CMOS NAND2 circuit and explain how one can calculate rise time and fall time using it for a capacitive load (C_L) at the output. 10

4. *(a)* Draw and explain the voltage and current transfer characteristics of a CMOS inverter. Derive the expression for static and dynamic power dissipation in the inverter circuit and discuss the ways of minimizing them. 10

(b) Draw the circuit diagram of BiCMOS NOT Gate and explain its working, advantages and disadvantages. 10

5. *(a)* What are Short-channel effects? Discuss the types of scaling and explain how they can address these effects and what are its limitations. 10

(b) Draw and explain the circuit diagram of a CMOS SRAM cell and compare its performance with that of a DRAM. 10

6. *(a)* Write the Verilog/VHDL code for designing full adder gate-level circuit using structural modeling. 10

(b) Draw and explain the block diagram of a typical programmable logic block. Discuss how many such blocks can be integrated to design a complex digital system. 10

7. (a) Discuss various steps in VLSI Design flow. 6

(b) Explain how any two-input boolean function can be implemented using a set of transmission gates. 6

(c) Draw and explain the logic gate diagram of PLA that can implement several SOP functions. 8