53 (EC 602) VLSI

2018

VLSI

Paper : EC 602

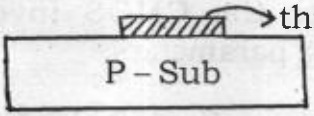
Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions out of **seven**.*

1. *(a)* Describe the lithographic sequences required for the following diagram (pattern). 6



(b) Write a short note on oxidation process. 4

(c) Derive the expression for Drain-to-Source current of an *n*-MOSFET biased in Triode mode and plot the $I_{DS} \sim V_{DS}$ characteristics. 10

2. *(a)* Draw the cross-bar switch matrix for 4-bit left and right rotation. 5+5

(b) Draw the cross-sectional view of Bi-CMOS technology. 4

(c) Implement the boolean function in CMOS logic $f(A, B, C) = \overline{A + (B.C)}$ and draw the lumped RC model for charging and discharging path. 2+2+2

3. *(a)* Describe the operation of 1 *bit* DRAM cell and compare its performance with 1 *bit* SRAM cell. 8+2

(b) Draw the CMOS sechmatics for a 2:1 MUX and corresponding layout. 2+4

(c) Describe the operation of n-MOS as a pass transistor. 4

4. *(a)* Consider the CMOS inverter with following parameters.

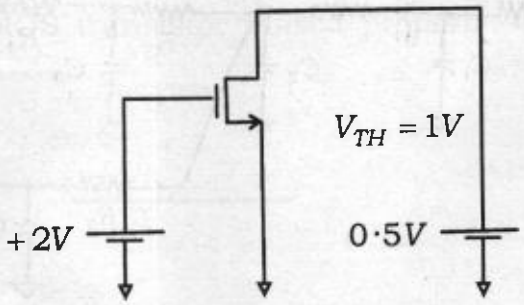
$$nMOS : V_{TH.N} = 0{\cdot}6V, \quad \mu_n C_{ox} = 60\,\mu A/v^2, \quad \left(\frac{w}{L}\right)_N = 8$$

$$pMOS : V_{TH.P} = 0{\cdot}7V, \quad \mu_p C_{ox} = 25\,\mu A/v^2, \quad \left(\frac{w}{L}\right)_p = 12$$

Calculate the value of switching threshold, if the supply used is 3·3*V*. 4

(b) Calculate the on-resistance of the MOS circuit shown below :

$$\left[\text{given } \mu_n C_{ox} = 100\mu\frac{A}{v^2},\ \left(\frac{W}{L}\right) = 10\right]$$

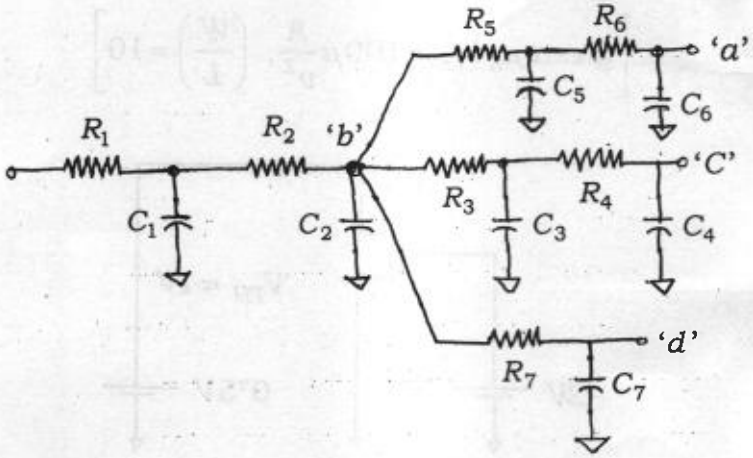


2

(c) Write short note on constant voltage scaling. 4

(d) Explain the operation of 2-4 *bit* binary numbers and draw the array base of multiplier architecture. 2+8

5. *(a)* Calculate Elmore's Delay for the following RC-tree shown as '*a*', '*b*', '*c*', '*d*'. 10



(b) Explain the logical implementation of 4 *bit* magnitude comparator with proper explanation. 10

6. *(a)* Describe the operation of 4 *bit* × 4 *bit* NOR based ROM array with circuit diagram. 10

(b) Draw the layout and schematic for the function $f(A, B, C) = \overline{(A + B).C}$ 6

(c) Describe the operation of a CMOS inverter. 4

7. *(a)* Draw and explain the fabrication steps for n-well CMOS process. 10

(b) Explain the logical implementation of Zero/one detector and its operation. 6

(c) Describe the inversion process of an *n*-MOS transistor biased properly. 4
