53 (EC 602) VLSI

2017

VLSI

Paper : EC-602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions out of **seven**.*

1. *(a)* Describe the fabrication steps for Bi-polar Technology of draw the layout of *n-p-n* Transistor by labelling each layer. 8+2

   (b) Describe the operation of 6T-SRAM cell and draw the layout of the cell. 8+2

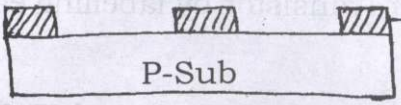
2. *(a)* Draw the CMOS implementation of a Full-Adder. 6

(b) Draw the layout of XOR and XNOR gate (2-input). 4

(c) List out the parasitic capacitance available in a MOS transistor and explain these capacitances with relevant expressions. Hence draw the small signal model of high frequencies. 2+6+2

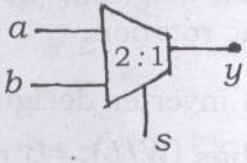
3. (a) Describe the operation of CMOS inverters and hence derive the expression for threshold voltage. 6+4

(b) Describe the lithographic sequences required to get pattern shown below. (With proper diagram) 6



(c) Write a short note on VLSI Design flow for digital circuit design. 4

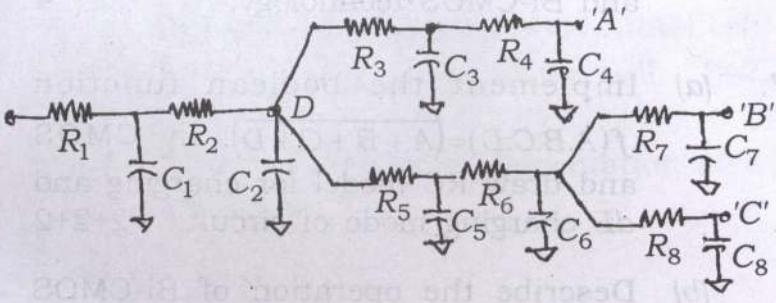
4. *(a)* Draw the CMOS implementation of its corresponding layout of the circuit shown below : 2+4



(b) Draw the diagram of an memory array. Explain the operation of 4bit × 4bit NOR based ROM array and draw the corresponding layout. 2+8+4

5. *(a)* Calculate the expressions for rise and fall time for a CMOS inverter. 10

(b) Calculate the Elmore's delay for the RC-tree shown below of the node : *'A', 'B', 'C', 'D'*. 10



6. *(a)* Explain the rotation operation for 4 bit binary number $B=b_3b_2b_1b_0$ with cross-bar switch diagram. (both left rotation and right rotation. 5+5

(b) A CMOS inverter designed in a CMOS process has $(W/L)_n=6$ and $(W/L)_p=8$ and the process parameters are as follows :

$K'_n=150\mu A/V^2$ $K'_p=62\mu A/V^2$

$V_{Tn}=0{\cdot}7V$ $V_{TP}=-0{\cdot}85V$

If the supply voltage used is $3{\cdot}3V$ and total output capacitance is $150\,fF$, then calculate the rise time and fall time and maximum signal frequency. 2+2+2

(c) Compare the performances of CMOS and Bi-CMOS technology. 4

7. *(a)* Implement the boolean function $f(A.B.C.D)=\overline{(A+B+C+D)}$ in CMOS and draw RC model for charging and dB charging mode of circuit. 2+2+2

(b) Describe the operation of Bi-CMOS inverter and discuss its problems. 10+4