

Total number of printed pages-4

53 (EC 602) VLSI

2014

VLSI

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

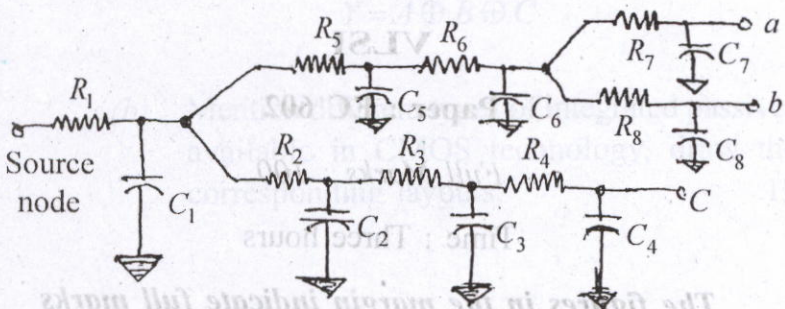
Section - A

Answer **any two** questions from question 2, 3, 4 and question 1 is **compulsory**.

1. (a) What do you mean by fringe-capacitance ?
How does it effect the delay in a circuit ? 2+2
- (b) Derive the expression for drain current (I_D)
in an n-MOS Transistor operating in Triode
region. 6
2. (a) Describe the operation of CMOS inverter,
draw the transfer characteristics. 10

Contd.

- (b) Calculate the Elmore's delay for the RC-tree shown below at nodes a , b , c . 10



3. (a) Write VHDL code for a full Adder using two Half Adders in structural model. 10

- (b) Describe the operation of BiCMOS inverter. 10

4. (a) Classify different types of memory and describe the operation of SRAM cell (6 Transistor). 2+8

- (b) Write short notes on photolithography and oxidation. 5+5

Section - B

Answer **any two** from question 5, 6, 8 & question 7 is compulsory.

5. (a) Describe channel length modulation for an n-MOS Transistor. Derive the expression of transition frequency (ω_T) for an n-MOS transistor in saturation. 4+6
- (b) Draw the layout for a CMOS inverter with proper substrate contacts. 6
- (c) Describe how n-MOS and p-MOS transistors can be used as pass transistors. 4
6. (a) Write down the fabrication steps for an n-well CMOS process with proper sketch. 10
- (b) Mention the basic blocks of an FPGA, draw the diagram of a typical FPGA Architecture. Discuss SRAM based FPGA in brief. 2+2+6
7. Why scaling is important in IC Design ? Mention the types of scaling. Describe the effect of scaling on I_{DS} , V_{TH} , C_{OX} . 2+2+6

8. (a) Draw the schematic diagram for the following boolean expression : 10

$$Y = \overline{A \oplus B \oplus C}$$

- (b) Mention different types of integrated passives available in CMOS technology, draw the corresponding layouts. 10