53 (EC 602) VLDG

2012C
2013
(May)

VLSI

Paper : EC 602

Full Marks : 100

Pass Marks : 30

Time : Three hours

The figures in the margin indicate full marks for the questions.

FIRST HALF

Answer ***any four*** *questions from* ***First Half.***

1. *(a)* Describe the fabrication steps for a 1-Poly 2-Metal n-well CMOS process, sequentially. 10

   (b) Describe the operation of a CMOS inverter, Plot the Voltage-Transfer-characteristics and find the inverter threshold voltage. 10

2. *(a)* Implement the the boolean expresion $y = A\overline{B} + \overline{A}B$ in CMOS technology and draw the complete layout with proper substrate contacts. 10

(b) Draw the layout of a CMOS inverter showing the minimum widths and spacings between each layer as specified in them. CMOS technology rules. 10

3. *(a)* Draw the Lamped-RC model of an interconnect and find the delay time. 5

(b) Draw the basic block diagram FPGA and describe the functionalities of each block. 10

(c) Describe briefly the operation of DMOS & PMOS as a pass transistor. 5

4. *(a)* Write short note on the lithography. Show each step required for patterning an oxide layer using positive photo-resist. 10

(b) What is scaling in CMOS technology ? Mention the types of scaling and discuss about the effects of scaling on circuit parameters. 10

5. *(a)* Derive the expression for figure of merit (W_0) for a CMOS technology. 5

(b) Describe the operation of Bi-CMOS inverter and how it is different from CMOS inverter. 10

(c) Draw the stick diagram for 2 input NOR gate implemented in CMOS technology. 5

6. *(a)* What is BIST ? Describe briefly the various techniques used for BIST. 12

(b) What do you mean by HDL Synthesis ? Write VHDL Code for a Full- Adder using two half-adders in structural model. 8

SECOND HALF

Answer all questions.

7. *(i)* *(a)* What is Probe Testing.

(b) Define Sheet Register and write the expression.

(c) How CVD oxide growth is different from native oxidation ?

(d) What do you mean by channel-length modulation and write expression for r_{ds}.

(e) Implement $y = A(B + C)$ in CMOS 5×2

(ii) Describe operation of nMOS inverter with depletion-load. 10
