53 (EC 602) DLDG

2014

VLSI

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Describe the fabrication steps for an n-well CMOS technology with neat sketch. 10

   (b) Describe the operation of a CMOS inverter and find the expression for inverter threshold. 5+5

2. *(a)* Implement the following logic function in CMOS. 5

$$y = \overline{(A \cdot B) + (C \cdot D)}$$

   (b) Draw the layout for the above logic circuit. 10

   (c) Explain in brief the use of P-MOS ϕn-MOS transistors as a pass gate. 5

3. *(a)* What is Bi-CMOS technology ? Draw the cross-sectional view of a typical Bi-CMOS technology. Write the advantages and disadvantages of Bi-CMOS technology in comparison to CMOS technology. 2+5+3

(b) What do you mean by Channel Length Modulation in a MOSFET transistor ? Describe. 5

(c) In a layout, the n-well layer used is of $1\mu m$ long, $500nm$ wide and $20nm$ thick, given the resistivity is $0{\cdot}008\Omega\text{-}cm$, find Sheet Resistance and Total Resistance. 5

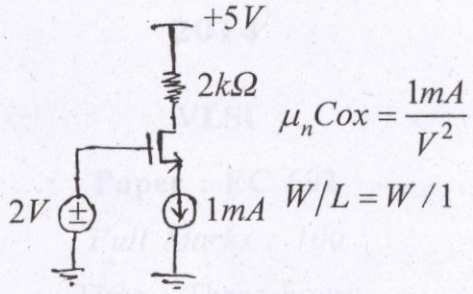
4. *(a)* Describe the operation of an SRAM cell with proper circuit diagram. 10

(b) Probe Testing is necessary in manufacturing integrated circuits. Explain why ? 5

(c) What you mean by Scaling ? Explain how I_{DS}, V_{TH}, C_{OX}, V_{DD} gets affected due to constant-field scaling. 5

5. *(a)* Describe the operation of a Bi-CMOS inverter and explain its problems. Why are improvements needed in the basic circuit to avoid these problems ? 8+2

(b) Given a circuit below : 10



Find the value of V_{GS}, V_{DS}, g_m and r_0

6. (a) Write VHDL code for implementing a 4:1 MUX using 2:1 MUXes in structural model. 10

(b) Describe the Built-in-Self-Test technique used in Testing integrated circuits. 10

7. (a) Design a full-Adder having inputs as A, B, C and output as sum and carry in CMOS logic and draw the schematic diagram. 10

(b) Write short note on oxidation. 5

(c) Write the lithographic steps required for patterning a poly in a nMOS technology. 5
