53 (EC 403) LICR

2019

LINEAR INTEGRATED CIRCUIT

Paper : EC 403

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions out of **seven**.*

1. *(a)* Describe the operation of a Phase-Locked Loop (PLL) using its block diagram. Mention its different operating modes. 8+2

   (b) Draw the circuit diagram for an integrator whose DC gain is finite and hence derive the expressions for –3*dB* frequency and unity gain frequency. 2+4+4

Contd.

2. (a) Draw the internal block diagram of 555 timer IC and explain the working principle. 2+8

(b) Explain the working of a Sigma-Delta ADC and mention how is it more advantageous to that of other ADC architectures. 8+2

3. (a) Design an Active (Butterworth 1st order) Low-pass filter with edge of passband frequency 10*kHz* and DC gain of 60*dB*. 5

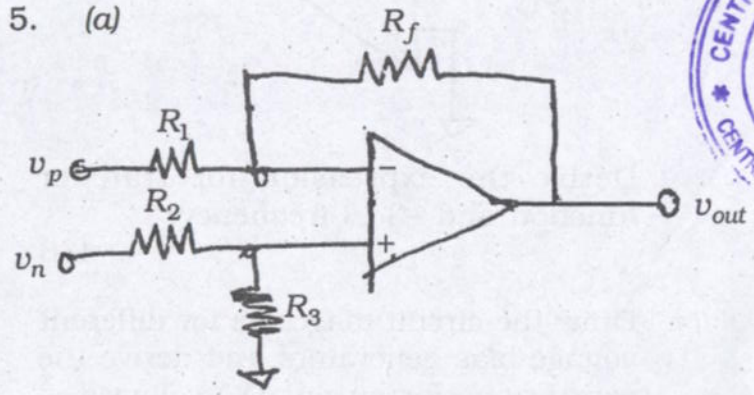
(b) Describe the astable operation using 555 timer. Hence derive its time period. 8+2

(c) Draw the circuit diagrams of different types of level shifters and write the output DC voltage levels. 5

4. (a) Derive the expressions for differential voltage gain for a dual-input unbalanced output (Active current mirror load). 10

(b) Draw the circuit diagram for a precision rectifier and explain its working. 10

5. (a)



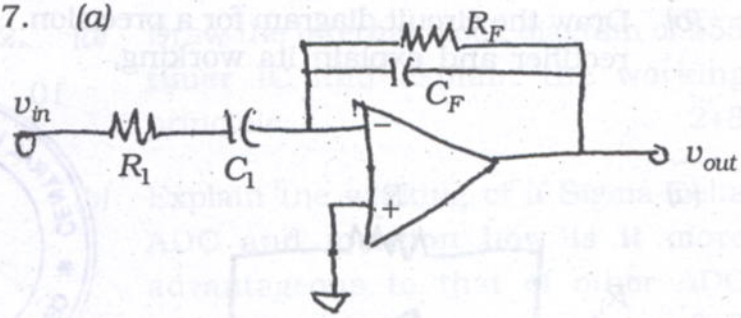
Derive the expression for differential gain and common mode gain. 5+5

(b) Describe the monostable operation of a 555 timer and derive the time period of its output. 8+2

6. (a) Describe the log and anti-log operation using op-Amp. 5+5

(b) Derive the differential and common mode gain for a dual-input balanced-output differential amplifier (BJT). 5+5

7. *(a)*



Derive the expression for transfer function and $-3dB$ frequency.

4+6

(b) Draw the circuit diagrams for different voltage bias generators and derive the expressions for output DC voltages.

10