

Total number of printed pages—4

53 (EC 403) LICR

2018

LINEAR INTEGRATED CIRCUIT

Paper : EC 403

Full Marks : 100

Time : Three hours

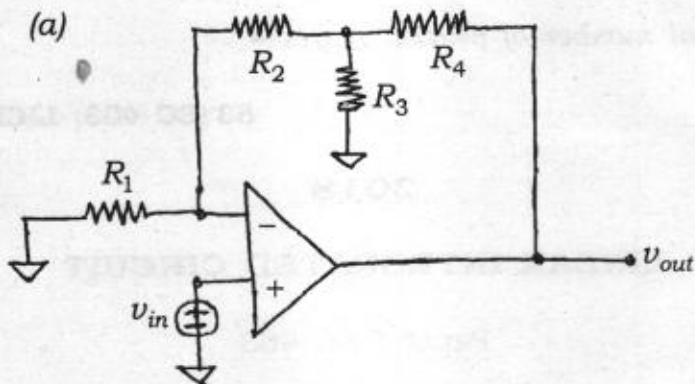
The figures in the margin indicate full marks for the questions.

Answer any five questions from seven.

1. (a) Derive the expressions for differential and common mode gain, hence discuss how CMRR can be improved for a dual input balanced output differential pair. 4+4+2
(b) What is the need of voltage bias generators and current bias generators in integrated Op-Amp circuits ? Discuss different circuits for each. 2+4+4

Contd.

2. (a)



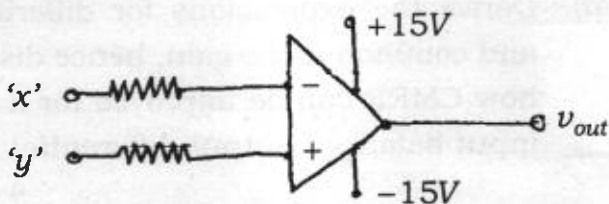
Assuming ideal op-amp, derive the expressions for the output voltage.

10

(b) Draw the internal schematic of a 741 Op-Amp (simplified), hence mention the various stages of it.

10

3. (a)



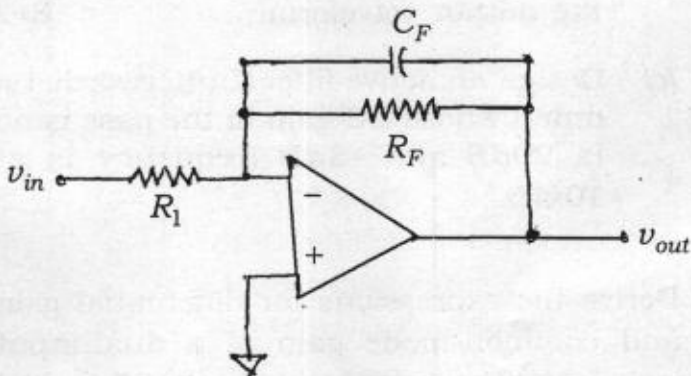
Draw the input and output waveforms, when 'x' signifies a triangular wave of 1kHz, $10V_{p-p}$ and 'y' signifies a sine wave of 100Hz, $6V_{p-p}$.

8

(b) Classify different types of multi-vibrators used for signal generation, hence discuss the generation of a square wave using a basic free-running multivibrator. 2+10

4. (a) Discuss the internal block diagram of a 555 timer and draw the circuit diagram for mono-stable mode. 8+2

(b)



Derive the expression for unity gain frequency and $-3dB$ frequency for the above circuit shown. 5+5

5. (a) Mention the different architectures of Analog-to-Digital converters and discuss briefly the SAR ADC. 2+8

- (b) Discuss the key operation of a phase-locked loop with proper block diagram and waveforms. 10
6. (a) Draw model of an ideal Op-Amp and a non-ideal Op-Amp showing different important parameters. 5
- (b) Describe the operation of 555 timer as an astable multivibrator, hence derive the expression for the time period of the output waveform. 8+2
- (c) Design an active filter (Butterworth 1st order) whose DC gain in the pass band is 20dB and -3dB frequency is at 10kHz . 5
7. Derive the expressions for differential gain and common-mode gain of a dual-input unbalanced output (Active load) differential pair. 10+10
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