53 (EC 401) DGEL

2021

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Explain the working of a standard TTL NAND with the help of circuit diagram. 6

   (b) For any logic family, describe the following terms briefly — Propagation delay, Fan-out and Noise margin. 6

   (c) Mention some advantages of a TTL circuit with open-collector. 3

   (d) Implement a two-input EX-OR in CMOS. 5

Contd.

2. *(a)* Implement the following Boolean expressions using NAND gates only — 4

(i) $Y = A \cdot B + \overline{A} \cdot \overline{B}$

(ii) $Y = \overline{A}(\overline{A} + B)$

(b) Minimize the following — 3+5=8

(i) $Y(A, B, C) = \Pi M(0, 1, 3, 7) \cdot \phi(5)$

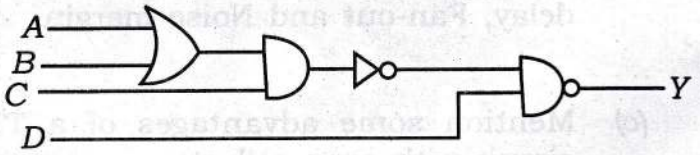
(ii) $Y(A, B, C, D, E)$
$= \sum m(1, 2, 3, 6, 8, 10, 21, 24, 31) + \phi(5, 15)$

(c) Perform the following operations using 2's complement arithmetic — 4

(i) (+ 40) – (+ 25)

(ii) (+ 15) – (– 18)

(d) Determine the O/P expression and truth table for the logic circuit shown below — 4



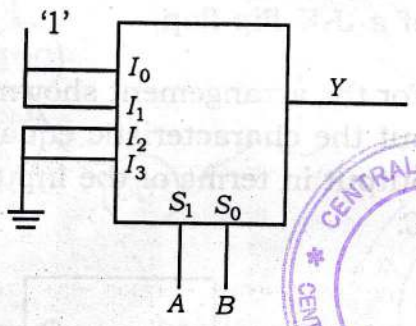
3. *(a)* What is a full-adder? Determine its truth table and logic circuit. 4

(b) Explain the working of a Four-Bit parallel adder-subtractor. 6

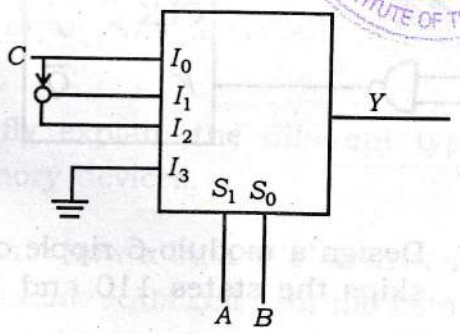
(c) What are parity generator and parity checker circuits? Briefly explain *any one* type with the help of its truth table and logic circuit. 6

(d) Find out the O/P expression for the following — 4

(i)



(ii)



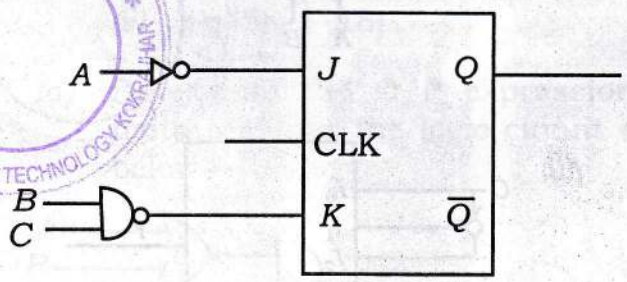
4. *(a)* Explain the working of a 3-to-8 line Decoder with the help of its truth table and logic circuit. 5

(b) Differentiate between Level-triggered and Edge-triggered flip-flops. 2

(c) Explain the working of an active HIGH S-R latch. 5

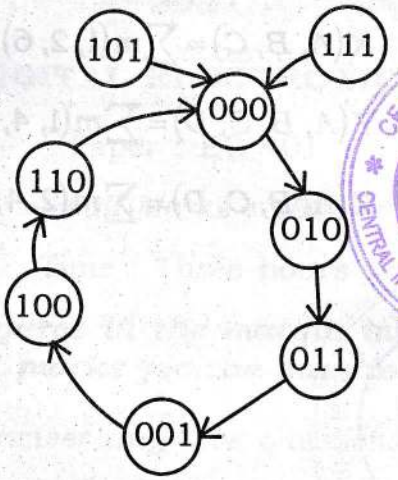
(d) Implement a D-flip-flop with the help of a J-K flip-flop. 5

(e) For the arrangement shown below, find out the characteristic equation for the output in terms of the inputs *A*, *B* and *C*. 3



5. *(a)* Design a modulo-6 ripple counter that skips the states 110 and 111. 6

(b) Design a counter using J-K flip-flops based on the state transition diagram shown below — 8



(c) Draw the timing waveforms for a Four-bit Serial-in-Serial-out shift register if the input data is (1010). 6

6. (a) Briefly explain the different types of memory devices. 4

(b) Explain how a binary '1' is written into a dynamic RAM cell with the help of its circuit diagram. 6

(c) Implement the following with a suitable PLA : 10

(i) $W(A, B, C) = \sum m(0, 1, 5)$

(ii) $X(A, B, C) = \sum m(1, 2, 6)$

(iii) $Y(A, B, C, D) = \sum m(1, 4, 6, 9)$

(iv) $Z(A, B, C, D) = \sum m(2, 4, 8, 12)$