53 (EC 401) DGEL

2019

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Draw the circuit diagram of TTL inverter and explain the transfer characteristics. Discuss the state of operation of each transistor in the circuit when the input voltage rise from *OV* to the maximum limit (V_{cc}). 8

   (b) What is the difference between fan-out and fan-in for a digital circuit ? Discuss how it is calculated by taking the example of any logic circuit. 6

Contd.

(c) Draw the circuit diagram of any CMOS logic gate circuit. Discuss why it has very low static power dissipation. Improve your circuit in order to introduce tri-state logic in it and explain its working. 6

2. (a) Convert the following: $4\times\frac{1}{2}=2$

(i) $(1000)_H = (\ )_{10}$

(ii) $(1010)_8 = (\ )_{10}$

(iii) $(101101.101)_2 = (\ )_{10}$

(iv) $(127.75)_{10} = (\ )_8$

(b) Using 8-bit 2's complement technique, perform the following operations– 4

(i) $(+18)+(-40)$

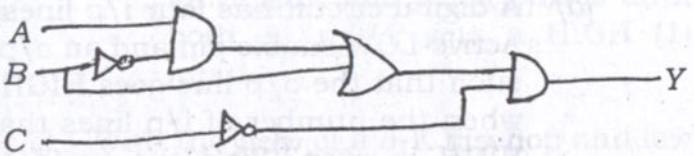
(ii) $(+16)-(+25)$

(c) Implement using only NAND gates 4

(i) $Y = AB + \overline{A}.\overline{B}$

(ii) $Y = (A+B)(A+\overline{C})$

(d) For the logic diagram, given below, answer the following questions: 4+4=8



(i) Find the expression and truth table for Y.

(ii) Minimize the expression if possible and implement using only NOR gates.

(e) Implement a buffer using only EX-OR gate and also prove it. 2

3. (a) Minimize with the help of K-map technique. 5

$$Y(A,B,C,D,E) = \sum m(0,1,2,3,14,15,30,31) + \phi(24)$$

(b) Implement with the help of 4:1 $M \cup X$ and few additional gates 5

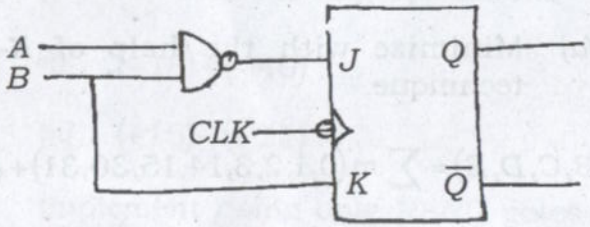
$$Y(A,B,C,D) = \sum m(1,4,6,10,12,13)$$

(c) Explain the working of a BCD adder with the help of proper block diagram. 5

(d) A digital circuit has four i/p lines, and Active-LOW enable pin and an o/p line, such that the o/p line goes HIGH only when the number of i/p lines that are HIGH is even. Find the truth table, o/p expression and logic diagram with minimum number of gates. 5

4. (a) Explain the working of a D-Latch with an Active-HIGH enable pin. 5

(b) For the diagram given below, answer the questions that follow : 4+4=8



(i) Find the characteristic table and the characteristic equation for Q_{n+1}

(ii) Assuming the present values as $A = 0$, $B = 0$ and $Q_n = 0$, show the output waveform for the flip-flop for *at least* four clock pulses until both A and B gets a HIGH (1) input.

(c) With the help of a J-K flip-flop and few additional gates, design a new flip-flop *(PQ)* based on the following requirements : 7

(i) when $P = 0, Q = 0$, flip-flop should reset

(ii) when $P = 0, Q = 1$, flip-flop should toggle.

(iii) when $P = 1, Q = 0$, flip-flop should reset.

(iv) when $P = 1, Q = 1$, flip-flop should set.

5. (a) What do you mean by modulus of a counter? Design a mod-10 asynchronous ripple counter that counts up starting from $(0000)_2$. 1+5=6

Contd.

(b) How many flip-flops will be required to design a counter for a home automation system to be able to count at least 200 people ? 2

(c) Design a synchronous counter with the help of D-flip-flops and additional gates that has the following sequence : 7

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 7 \rightarrow 0$

(d) Explain how registers can be used for data transfer applications by giving example of *any one* type. 5

6. (a) Differentiate between : 2+2=4

(i) ROM and PROM

(ii) Static RAM and Dynamic RAM

(b) Draw the circuit diagram of a capacitor and MOSFET based Dynamic RAM cell and explain clearly how a Binary '1' or '0' is written to the memory cell. 10

(c) Implement the Boolean functions given below with a suitable PROM. 6

$Y_1 = \sum m(0,1,2)$

$Y_2 = \sum m(2,6,7)$

7. (a) Write the program table to implement a 4-bit binary to gray converter using a PLA and show the arrangement for the same. 12

(b) Write *two* differences between PLDs and FPGA. 2

(c) Briefly explain *any two* Programmable Interconnect Technologies used for PLDs, FPGA etc. 6