53 (EC 401) DGEL

2018

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Convert the following — 4×0·5=2

   (i) $(23{\cdot}15)_{16}$ to Binary

   (ii) $(84{\cdot}25)_{10}$ to Octal

   (iii) $(101011)_2$ to Gray

   (iv) $(11000{\cdot}011)_2$ to Octal

   (b) Perform the following operations using 2's complement arithmetic — 4

   (i) (+45) + (–19)

   (ii) (+32) – (+18)

Contd.

(c) Implement EX-OR and EX-NOR gates using only NOR gates. 4

(d) For the circuit given below, answer the following — 2+2+2=6

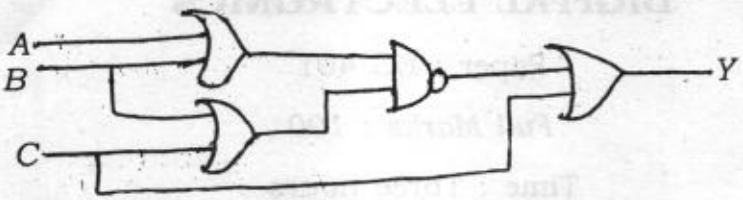

Fig : (1)

(i) Expression for Y and simplify

(ii) Truth table

(iii) Implement the simplified expression using only NAND gates.

(e) Simplify the following Boolean expressions — 2+2=4

(i) $\left[A\overline{B}(C+BD)+\overline{A}\,\overline{B}\right]C$

(ii) $\overline{AB+AC}+\overline{A}\,\overline{B}C$

2. (a) Find the simplified expression for the following using K-map technique and implement the same using basic gates. 4+6=10

(i) $Y(A,B,C,D)=\pi M(1,2,5,6,7,13,14)+\phi(0,3,15)$

(ii) $F(A, B, C, D, E)$

$= \sum m(0, 1, 2, 4, 5, 6, 13, 16, 17, 18, 20, 21, 22, 31)$
$+ \phi(8, 9, 10, 11, 30)$

(b) Explain the working of a Carry Propagation Lookahead Carry Generator for a 4-bit parallel binary adder. 6

(c) A digital circuit has two *i/p* lines and four *o/p* lines such that, the o/p lines are used to turn ON/OFF four LEDs. Design the logic circuit so that at least one LED is turned ON depending on the status of *i/p* lines but no two LEDs should be turned on simultaneously. 4

3. (a) Implement the given Boolean Expression using a 4 : 1 MUX — 5

$$Y = ABC + A\overline{B} + \overline{B}C$$

(b) Implement a Full-Adder using a 3-to-8 decoder and external NOR gates. 5

(c) Find out the Boolean Expression for the following — 2+3=5

(i)

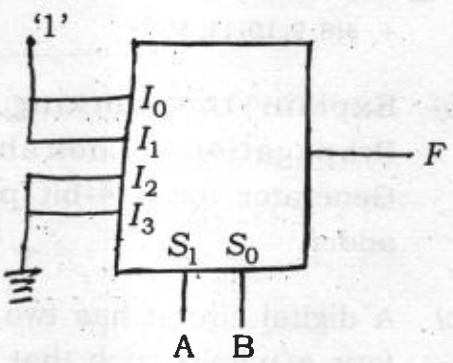

Fig. (2·1)

(ii)

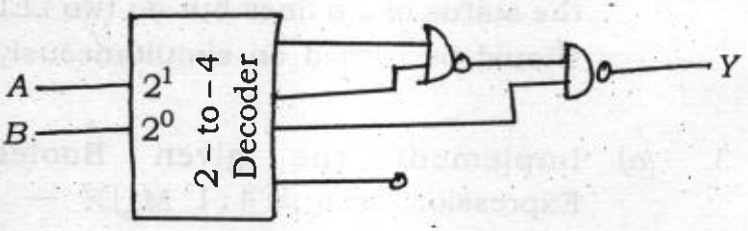

Fig. (2·2)

(d) Explain the construction and working of an Active HIGH J-K flip-flop. 5

4. *(a)* Consider an Active HIGH J-K flip-flop shown Below, and answer the questions that follow — 5+5=10

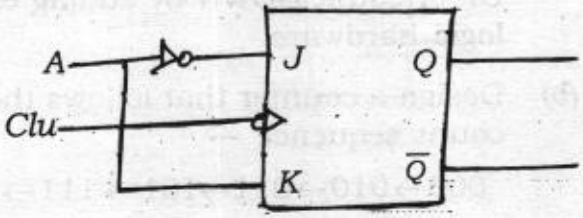

Fig.(3)

(i) Find out the characteristic table and characteristic equation for Q_{n+1} in terms of *A*.

(ii) Show the o/p wave form for 'Q' if the q/p 'A' changes its state to low (assuming it was HIGH permanently)

(b) The excitation table of a flip-flop 'AB' is given as — 10

Q_n	Q_{n+1}	*A*	*B*
0	0	*X*	1
0	1	*X*	0
1	0	0	*X*
1	1	1	*X*

Use this 'AB' flip-flop to construct a D-flip-flop.

5. *(a)* Explain the working of a 4-bit ripple counter with necessary diagram and also show how it can be used to count UP or count DOWN by adding external logic hardware. 10

(b) Design a counter that follows the given count sequence — 8

$$000 \rightarrow 010 \rightarrow 011 \rightarrow 101 \rightarrow 111 \rightarrow 000$$

(c) Differentiate between Asynchronous and Synchronous Counters. 2

6. *(a)* Realize the following equations with a suitable PLA. 12

$$W(A,B,C,D) = \sum m(0,1,5,9,12)$$
$$X(A,B,C,D) = \sum m(1,2,3,9,10)$$
$$Y(A,B,C,D) = \sum m(4,5,12)$$
$$Z(A,B,C,D) = \sum m(2,3,6,9)$$

(b) Explain how D-flip-flops are used to constant an n-bit register with an example and necessary diagram. 8

7. Write short notes on : ***(any four)*** 4×5=20

(i) TTL

(ii) ECL

(iii) BCD to Seven Segment Decoder

(iv) Magnitude Comparator

(v) Binary Codes

(vi) Memory Devices.
