53 (EC 401) DGEL

2017

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Perform the following operations using 2's complement arithmetic. 2+2=4

   (i) $(+37)+(-18)$

   (ii) $(+24)-(+14)$

   (b) For the logic circuit shown below, answer the following : 2+2+4=8

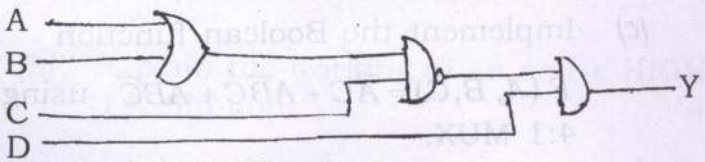

Figure 1

(i) Draw the truth table

(ii) Find out the expression for Y and simplify

(iii) Implement the same using only 2-input NAND gates.

(c) Simplify the following Boolean expressions — 2+2=4

(i) $\left[A\overline{B}\,(C+BD)+\overline{A}\cdot\overline{B}\right]C$

(ii) $\overline{AB+AC}+\overline{A}\overline{B}C$

(d) Minimize using K-map.

$$Y(A,B,C,D)=\sum m(0,2,3,8,10,12)+\phi(6,9,15)$$ 4

2. (a) Design a full-adder using two half-adders and explain its working. 4

(b) Using full-adders, design a circuit that is capable of performing both 4-bit binary addition as well as subtraction. 5

(c) Implement the Boolean function $F(A,B,C)=\overline{A}C+A\overline{B}C+AB\overline{C}$ using a 4:1 MUX. 3

(d) Determine the function performed by the following circuit. Also, what will be the output (Y) if $S_1 = 1$ and $S_0 = 0$? 3

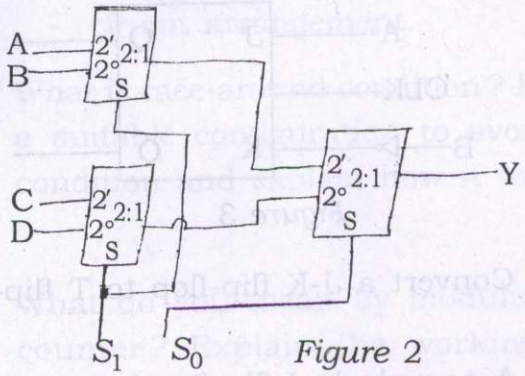

Figure 2

(e) Implement a Full-subtractor using 2×4 decoders and some basic gates if required. 5

3. (a) Differentiate between — 6

(i) Synchronous and Asynchronous inputs

(ii) Level and Edge triggered flip-flops

(iii) D-latch and D-flip-flop.

(b) Explain the working of an active HIGH J-K flip-flop. 4

(c) Consider a J-K flip-flop shown below. Find out its characteristic table and write the characteristic equation for Q_{n+1} in terms of A and B. 4

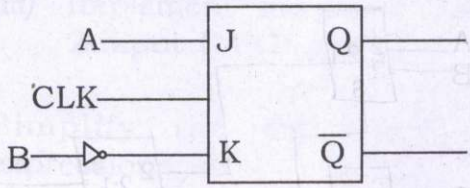

Figure 3

(d) Convert a J-K flip-flop to T flip-flop. 6

4. (a) A new clocked flip-flop has two inputs X and Y in addition to the clock input. The flip-flop functions as follows — 2+2+6=10

If XY=00, the flip-flop changes state with each clock pulse

If XY = 01, the output Q becomes '1' with the next clock pulse

If XY = 10, the output Q becomes '0' with next clock pulse

If XY = 11, the output Q retains its state.

(i) Write the characteristic table for the XY flip-flop

(ii) Write the excitation table for the flip-flop

(iii) Show the necessary steps required to implement this XY flip-flop using a J-K flip-flop and draw the circuit arrangement.

(b) What is race-around condition ? Provide a suitable configuration to avoid this condition and explain how it works. 5

(c) What do you mean by modulus of a counter ? Explain the working of a 4-bit binary ripple counter. 5

5. (a) Differentiate between asynchronous and synchronous counters. 2

(b) Determine the number of flip-flops required to design a counter that is capable of counting upto 4000 items. 2

(c) Design a 3-bit counter which counts in the following sequence — 8

$0 \rightarrow 3 \rightarrow 6 \rightarrow 1 \rightarrow 4 \rightarrow 7 \rightarrow 2 \rightarrow 5 \rightarrow 0 \rightarrow 3 \ldots$ etc.

(d) The following table gives an excitation table of a certain flip-flop having A and B as inputs. Use this flip-flop to design a MOD-5 synchronous counter that follows the sequence $0 \rightarrow 1 \rightarrow 3 \rightarrow 5 \rightarrow 7$ and resets to 0 at the end of sequence. Also, the counter should reset itself to .0 whenever its goes to unwanted state.

Present State (Q_n)	Next State (Q_{n+1})	A	B
0	0	0	0
0	1	0	1
1	0	1	x
1	1	x	1

Table 1 8

6. (a) Design an Excess-3 to BCD code converter using suitable PLA or PAL. 8

(b) Implement the following Boolean functions using suitable PAL —

$W(A, B, C) = \sum m(0, 1, 2, 4, 6)$

$X(A, B, C) = \sum m(0, 2, 6, 7)$

$Y(A, B, C) = \sum m(3, 6)$

$Z(A, B, C) = \sum m(1, 5, 7)$ 8

(c) Differentiate between — 4

(i) ROM and RAM

(ii) Static RAM and Dynamic RAM.
