53 (EC 401) DGEL

2014

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Convert the following decimal numbers to binary and excess–3 code. 4

   (i) $(123)_{10}$ *(ii)* $(738)_{10}$

   (b) State and prove De Morgan's theorem. Simplify the following Boolean equations using Boolean algebra and draw the simplified logic circuit. 3+5=8

   (i) $F = AB + A(B + C) + B(B + C)$

   (ii) $f = (A, B, C, D, E) = (AB + C + D)(\overline{C} + D)(\overline{C} + D + E)$

(c) Describe the operation of Fulladder and Half subtractor. 8

2. (a) Design the logic circuit to generate an even parity generator and checker for 3-bit binary inputs. 8

(b) Minimize the following expressions using K-maps and implement it 12

(i) $Y(A,B,C,D)=\sum m(1,2,5,6,8,9)$

(ii) $Y(A,B,C,D)=\Pi m(0,1,2,3,8,9,10,11,12,13)$

(iii) $Y(A,B,C,D)=\sum m(0,1,3,7)+d(2,5)$

3. (a) Design the following code converters : ***(any two)*** 2×5=10

(i) Binary to Gray

(ii) Binary to Excess-3

(iii) Exlcess-3 to BCD.

(b) Draw a neat circuit diagram of clocked *J-K* flip-flop using NAND gates. Give its truth table and explain race-around condition. 10

4. (a) Explain how a *J-K* flip-flop is converted into *D* flip-flip and *T* flip-flop. 10

(b) Explain what you understand by a register. Describe the working of a serial in serial out shift register. 10

5. (a) Design and implement a $Mod-5$ synchronous counter using $J-K$ flip-flop. 8

(b) Design a circuit to generate the sequence $0 \rightarrow 2 \rightarrow 5 \rightarrow 4 \rightarrow 7 \rightarrow 3$. 7

(c) Explain the Design procedure for sequential logic circuits. 5

6. (a) Design a $4K \times 8$ memory chip using $2K \times 8$ chips. 8

(b) Differentiate static RAM and dynamic RAM. 5

(c) Realize the following equations with a suitable PLA. Draw the logic diagram using PLA. 7

$$F_1(A,B,C,D)=\sum m(3,7,8,9,11,15)$$

$$F_2(A,B,C,D)=\sum m(3,4,5,7,10,14,15)$$

$$F_3(A,B,C,D)=\sum m(1,5,7,11,15)$$

7. Write short notes on : ***(any two)*** 2×10=20

(i) Programmable Logic Devices

(ii) Multiplexer and Demultiplexer

(iii) Flip-Flop

(iv) Expanding word size and word capacity.
