Total number of printed pages-4

#### 53 (EC 401) DGEL

## **2012 C 2013** (May)

## DIGITAL ELECTRONICS

Paper : EC 401 Full Marks : 100 Pass Marks : 30 Time : Three hours

# The figures in the margin indicate full marks for the questions.

Answer any five questions.

- 1. (a) Express the following decimal numbers in the XS-3 code. 3
  - *(i)* 2515 *(ii)* 653
  - (b) Minimize the following expression using K-map

 $Y(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 6, 7, 11, 13, 14)$ 

Contd.

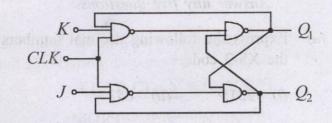
(c) Design a 5-bit odd parity generator. Draw and explain the carry look-ahead adder.

5+7=12

- 2. (a) Design a 2-bit comparator using logic gates.
  - (b) What is multiplexer? Implement the following function using 8 : 1 MUX.

$$f(A, B, C, D) = \sum m (2, 4, 5, 7, 10, 14)$$
  
3+8=11

- (c) Distinguish between combinational and sequential circuits.
- 3. (a) Identify Q and  $\overline{Q}$  outputs of the clocked J-K flip-flop shown in figure below : 4



- (b) Draw the logic circuit of J-K flip-flop using T-flip-flop.
- (c) Design a MOD-5 synchronous counter using T-flip-flop. 10

2

53 (EC 401) DGEL/G

- 4. (a) What is register ? Describe the working of a
   4-bit SISO shift register and draw the waveforms of shift register for serial input.
   3+7=10
  - (b) Design a sequential generator using J-K flip-flop to generate the sequence. 10

 $0 \rightarrow 2 \rightarrow 4 \rightarrow 5 \rightarrow 1 \rightarrow 7 \rightarrow 6$ 

5. (a) For a memory with M words storage, find the number of pins required for addressing and range in binary format for each of the following cases.

(i) 
$$M = 64$$
 (ii)  $M = 16$  5

- (b) State the relative merits of static and dynamic RAMs. 5
- (c) State the full name of the following memory devices and describe very briefly the function of *each one.*
  - (i) ROM (ii) EPROM
- 6. (a) Explain CMOS inverter gate with a circuit diagram. 5

### 53 (EC 401) DGEL/G

3

Contd.

- (b) Explain the basic ECL OR / NOR gate with a neat circuit diagram. Why does the ECL family have the lowest propagation delay of all logic families?
  - (c) When does a TTL circuit act as a current source? As a current sink? 5
- 7. (a) Draw the block diagram of PLA and write the applications of PLA. 5
  - (b) Realize the following equations with a suitable PLA and draw the logic diagram using PLA.

(i) 
$$f_1(A, B, C, D) = A\overline{B}D + \overline{A}B\overline{D}$$
  
 $f_2(A, B, C, D) = A + B\overline{D}$ 

(ii) 
$$W(A, B, C) = \sum m(0, 1, 4)$$
  
 $X(A, B, C) = \sum m(0, 3, 4, 7)$   
 $Y(A, B, C) = \sum m(1, 2, 6)$   
 $Z(A, B, C) = \sum m(2, 3, 6, 7)$ 

53 (EC 401) DGEL/G

4

200

6

9