53 (EC 301) ELDC

2019

ELECTRONIC DEVICES & CIRCUITS

Paper : EC 301

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* *(i)* Discuss the effect of Q-point location on ac operation. 3

(ii) Write down the application of CC amplifier. 1

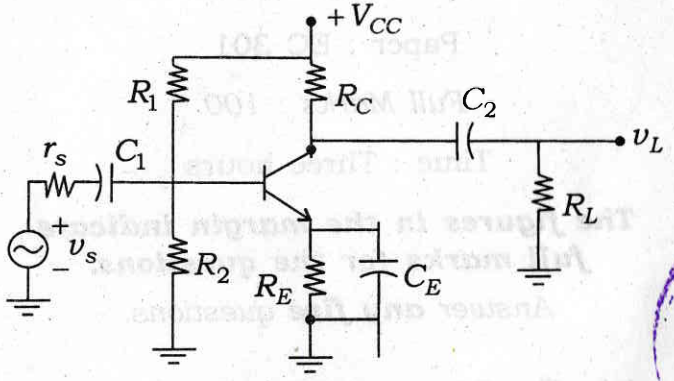
(iii) Draw the small-signal model of the CB configuration. 2

(b) *(i)* Compare voltage gain, current gain, input resistance, output resistance in between three different configurations (CC, CB, CE). 2

Contd.

(ii) What are the functions of coupling capacitor in a single stage complifier ? 2

(c)

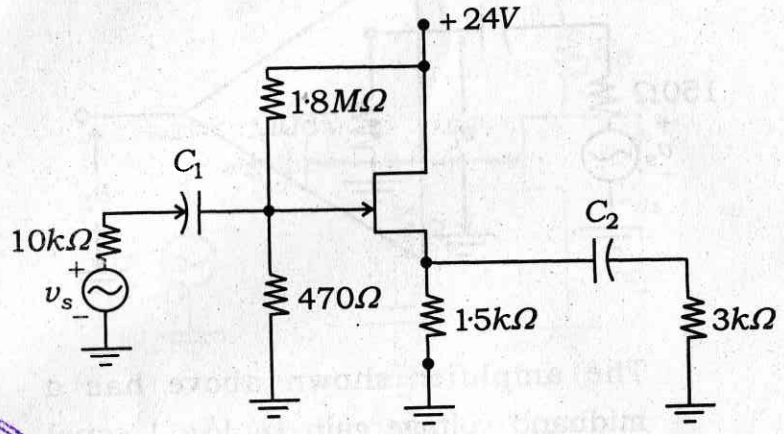


For the above circuit :

(i) Draw the equivalent ac circuit with small signal CE model. 4

(ii) Calculate input resistance (r_i), current gain (A_i), voltage gain (A_v), overall voltage gain, overall current gain $\left(\frac{i_L}{i_s}\right)$. 6

2. (a)



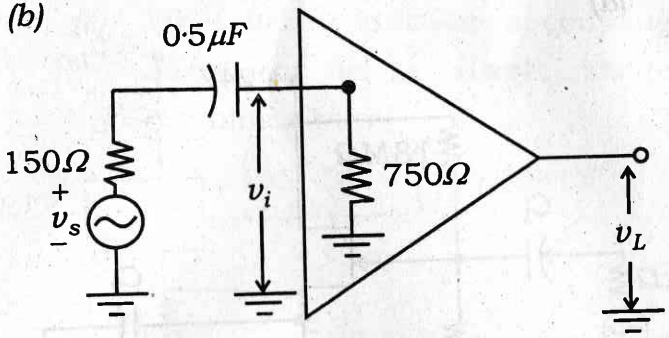
The JFET above has $g_m = 5 \times 10^{-3}$ s and $r_d = 100k\Omega$.

Find (i) the input resistance

(ii) the voltage gain

(iii) the output resistance of the amplifier.

(b)



The amplifier shown above has a midband voltage gain $|v_L|/|v_S|$ equal to 90. Find 5

(i) the voltage gain $|v_L|/|v_i|$

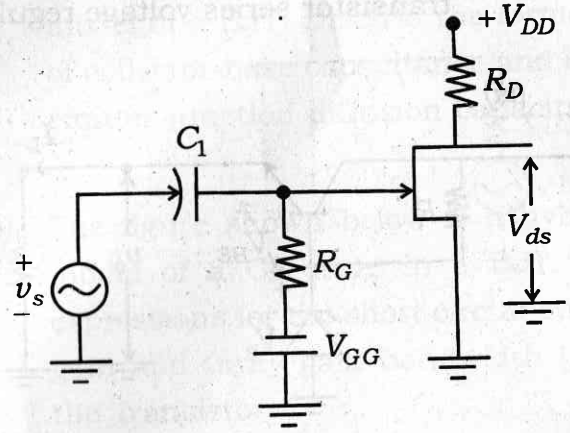
(ii) the lower cutoff frequency

(iii) the voltage gain $|v_L|/|v_s|$ in dB, at the cutoff frequency.

(c) (i) Explain how the shunt capacitance affects the high frequency response of an amplifier. 3

(ii) What is the source of this shunt capacitance ? 1

(d)



(i) Draw the small signal equivalent circuit of the above amplifier and find out voltage gain equation. 4

(ii) Draw & discuss different types of Amplifier Models. 2

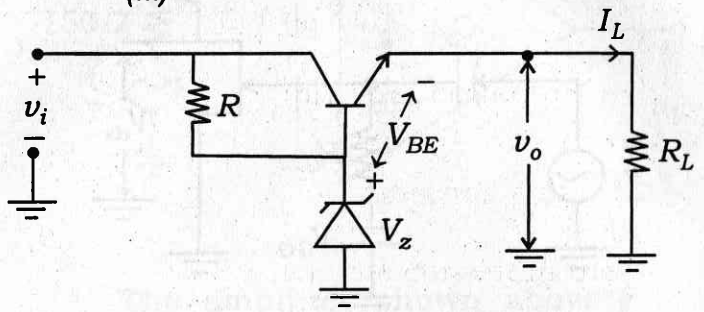
3. (a) (i) What are different methods of Interstage Coupling. Discuss each type in brief. 4

(ii) State and explain Miller's theorem. 2

(b) (i) Draw & explain block diagram of a series voltage regulator. 5

(ii) Draw and explain the circuit of a transistor series voltage regulator. 4

(iii)



In the above Figure

$V_i = 20V$ $R = 200\,\Omega$ $V_z = 12V$

$V_{BE} = 0{\cdot}65V$

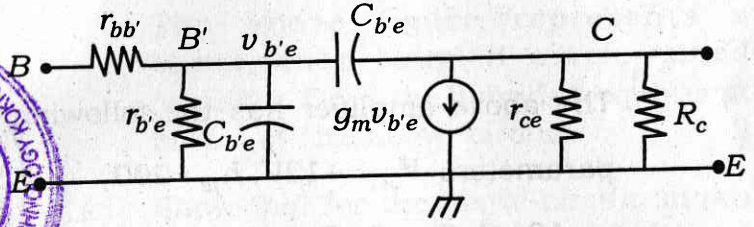
Find (a) V_0

(b) The collector emitter voltage of the pass transistor and

(c) the current in the 200Ω resistor. 5

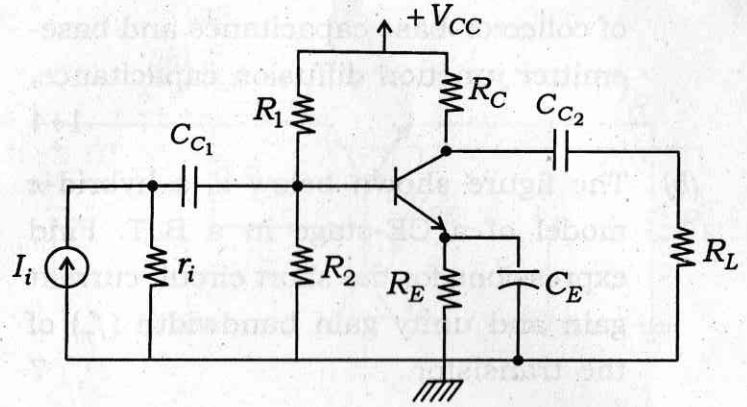
4. (a) Draw the hybrid-π or the Giacoletto-π model of a BJT. Discuss the formation of collector-base capacitance and base-emitter junction diffusion capacitance. 1+4

(b) The figure shown below is a hybrid-π model of a CE-stage in a BJT. Find expressions for the short circuit current gain and unity gain bandwidth (f_T) of the transistor. 7



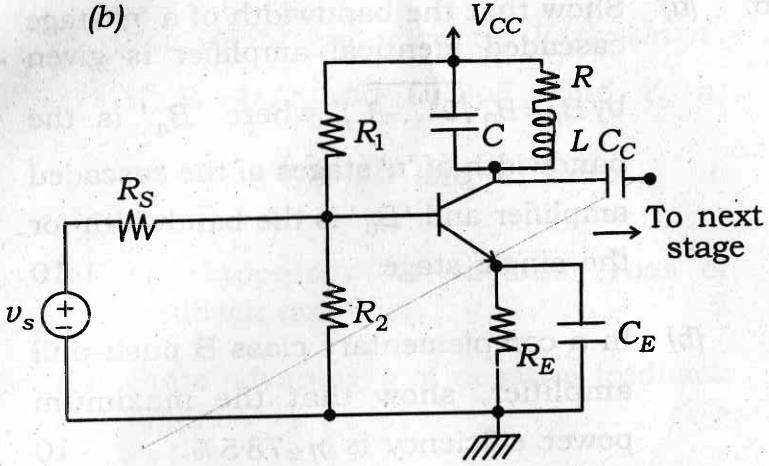
(c) The following low-frequency parameters are known for a given transistor at room temperature, and at $I_c = 10mA$ and $V_{CE} = 10V$, $h_{ie} = 500\Omega$, $h_{oe} = 4\times10^{-5}\,A/V$; $h_{fe} = 100$; $h_{re} = 10^{-4}$. At the same operating point, $f_T = 50\,MHz$ and $C_{b'c} = 3pF$. Calculate the values of all the hybrid-π parameters. 8

5. *(a)* 10



The above amplifier has the following parameters $V_{CC}=+12V$, $h_{fe}=200$; $r_i=10k\Omega$, $C_{b'c}=2pF$, $R_b=R_1 \,||\, R_2=2k\Omega$; $C_{b'e}=200pF$, $r_{bb'}=20\Omega$, $r_{b'e}=150\Omega$, $R_L=200\Omega(R_C>>R_L)$. Draw the hybrid-π model and hence find the mid-band gain, $3dB$ frequency f_H.

(b)



The above figure represents a capacitance coupled single tuned amplifier. Draw the hybrid-π equivalent model of the above circuit. 2

(c) Show that for the above circuit shown in *(b)*, the voltage gain (without considering the source resistance R_s) is given by

$$A_V=\frac{A_{res}}{1+j2\delta Q_e}$$; where

$\delta \rightarrow$ Fractional frequency variation,

$Q_e \rightarrow$ Effective quality factor of the o/p circuit.

$A_{res} \rightarrow$ Voltage gain at resonance $(\delta=0)$. 8

6. *(a)* Show that the bandwidth of a '*n*' stage cascaded identical amplifier is given by $B_n = B_0\sqrt{2^{1/n}-1}$; where 'B_n' is the bandwidth of '*n*' stages of the cascaded amplifier and 'B_0' is the bandwidth for the single stage. 10

(b) In a complementary class B push-pull amplifier, show that the maximum power efficiency is $\eta \simeq 78{\cdot}5\%$. 10

7. *(a)* Define the following : 3

(i) Offset voltage

(ii) CMRR

(iii) Slew Rate

(b) Derive the expression of 3-input inverting summing amplifier. 5

(c) Draw the circuit of an integrator and derive the expression for its output voltage. State application of an integrator. 6

(d) For an integrator circuit $V_i(t) = \sin \omega t$.

If $R_1 = 4k\Omega$ and $C = 2\mu F$, find V_0 at $\omega t = \frac{\pi}{2}$ if $V_0(0) = 0$ and $\omega = 1MHz$. 6

8. *(a)* Give topology for various types of feedback amplifier. 2

(b) State advantages of negative feedback amplifier. 3

(c) Explain the effect of negative feedback on lower cutoff and upper cutoff frequency of the amplifier and prove that bandwidth with feedback is greater than bandwidth without feedback. 10

(d) An amplifier has midband voltage gain of 1000 with $f_L = 50Hz$ and $f_H = 50kHz$. If 5% feedback is applied then calculate gain f_L and f_H with feedback. 5

9. *(a)* Differentiate between class *A*, *B* and *C* amplifier. 3

(b) Explain the working of directly coupled class *A* amplifier with the help of neat diagram. 6

(c) Maximum collector efficiency of class A amplifier is ———. 1

(d) Describe Hartley oscillator with its operation. 6

(e) Find the operating frequency of a transistor Hartley oscillator, if $L_1=100\mu H$, $L_2=1mH$, mutual inductance between the coils is $20\mu H$ & $C=20pF$. 4

10. (a) Differentiate between JFET and BJT. 4

(b) Explain operation of *N*-channel FET. Also explain its static characteristic curves. 8

(c) A JFET has a drain current of $5mA$. If $I_{DSS}=10mA$ and $V_{GS(off)}=-6V$, find the value of V_{GS} and V_P. 3

(d) Draw a neat circuit diagram of transistor monostable multivibrator and discuss its working. 5