(DIGITAL ELECTRONICS-DIE304)
End Term Examination-*2024*
Full Marks- 100: Time- 3 Hours

Answer question no. 1 and any four (4) questions from the rest.

1. a) Fill up the blanks- 10 x 1 = 10

i) The hexadecimal number that comes after $(FAFF)_{16}$ is _____

ii) Octal Number that comes before $(6700)_8$ is _____

iii) 2's complement of decimal number $(7)_{10}$ in binary is _____

iv) The output of a 6-input Ex-OR gate for the input 111001 will be _____

v) The dual of the Boolean Expression- $(\bar{A}.B + A.C).\bar{B}$ is _____

vi) Canonical form of the Boolean Expression- $A + BC$ is _____

vii) Octal number equivalent of $(FA07)_{16}$ is _____

viii) 2 Megabytes is equal to _____ bits.

ix) A multiplexer having 100 input lines should have a minimum of _____ select lines.

x) If the input of a J-K flip-flop is (0,0), its output will be _____ after the next clock pulse. (Qn = 1)

b) Multiple choice questions- 5 x 1 = 5

i) Which of the following logic gates has the output expression equivalent to- $Y = \bar{A}B + A\bar{B} + AB$

[A] AND [B] OR [C] NAND [D] NOR

ii) If one of the inputs of an Ex-OR gate is permanently tied to logic '1', then-

[A] Output will be LOW [B] Output will be HIGH

[C] Act like a buffer [D] Act like a NOT gate

iii) Addition of a 2's complement of a binary number X to binary number Y yields-

[A] X + Y [B] X – Y [C] Y – X [D] None

iv) Minimum number of half-adders required to add two 4-bit data is-

[A] 4 [B] 5 [C] 6 [D] 7

v) Which of the following is an invalid BCD code?

[A] 0011 [B] 1001 [D] 1100 [D] 0111

c) Answer the following questions- 5 x 1 = 5

i) 'NAND gate is called a Universal gate'. Justify the given statement.

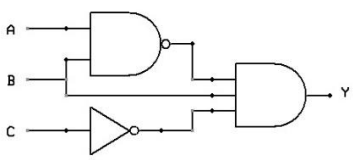
ii) State the De-Morgan's theorems.

iii) Name any one difference between combinational and sequential digital circuits.

iv) What is a magnitude comparator?

vi) Differentiate between level-triggered and edge-triggered flip-flops.

2. a) For the logic circuit diagram given below, write its output expression and the truth table. 5



b) Implement an OR gate using NAND gates only. 2

c) Prove that- i) $X.(X + Y) = X$ ii) $(\overline{X} + Y).Y = X.Y$ iii) $(A + B).(A + \overline{B}) = A$ 3 x 2 = 6

d) Minimize the following Boolean Expressions- 2 x 2 = 4

i) $Y = \bar{A}.B.C + A.\bar{B}.C + A.B.\bar{C} + A.B.C$

ii) $Y = (A + B + \overline{C})(A + B + C)(\overline{A} + B + C)$

e) Draw the logic circuit diagram and truth table for the Boolean expression- $Y = A + B\bar{C}$ 1 + 2 = 3

3. a) Minimize using K-Map technique, write the minimized expression and draw the logic circuit diagram- 4 + 6 = 10

i) $F(A, B, C) = \sum m(0,1,2,6,7) + \sum d(3)$

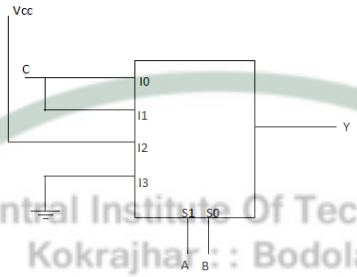
ii) $F(A, B, C, D) = \sum m(4,5,6,7,13,14,15) + \sum d(0,1,11)$

b) Explain the working of a Full-adder circuit with the help of its truth table and logic diagram. 4

c) Explain the working of a 4-bit binary adder with its functional block diagram. 6

4. a) What is a multiplexer? Implement an 8:1 multiplexer using two 4:1 multiplexers. 2 + 4 = 6

b) 4



For the 4:1 Mux shown above, find the output expression for Y.

c) Explain the working of a 3-to-8-line Decoder. 6

d) Implement a full-subtractor with a 3-to-8-line decoder and a few additional gates. 4

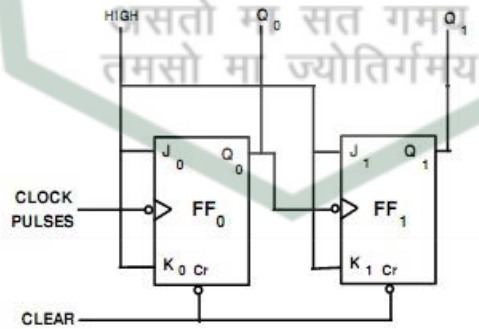
5. a) Explain the working of an Active-Low S-R Latch. 4

b) Construct a clocked J-K flip-flop using NAND gates and state its characteristic table. 6

c) If both the inputs of a negative-edge-triggered J-K flip-flop is permanently HIGH, draw the output waveform for the flip-flop for at least 4 clock pulses. Also, find out the frequency and time-period of the output waveform if the frequency of the clock input is 2 KHz. 4 + 2 = 6

d) What do you mean by race-around condition in J-K flip-flop? State how this condition can be avoided. 2 + 2 = 4

6. a) For the flip-flop configuration provided below, answer the questions that follow. 2 + 6 + 2 = 12



i) What will be the outputs at Q_0 and Q_1 if CLEAR input is permanently grounded?

ii) If CLEAR = 'HIGH', draw the output waveforms of Q_0 and Q_1 for at least 6 clock pulses. (Assume both Q_0 and Q_1 = 0 initially).

iii) If the input Clock pulse has a frequency of 4 Hz, what will be the frequencies of Q_0 and Q_1 respectively?

b) Implement the Boolean function with Y (A,B,C) = ∑m(0,2,6,7) a suitable multiplexer. 4

c) Implement a T-flip-flop using a J-K flip-flop. 4