Total number of printed pages: 3

DIPLOMA (D) / III / DIE304

2023

DIGITAL ELECTRONICS

Full Marks: 100

Time: Three hours

The figures in the margin indicate full marks for the questions.

Answer all the questions.

1. a) Convert the following numbers- 10 x 1 = 10

   i) $(17)_8$ to Decimal ii) $(45)_2$ to Hex

   iii) $(1001101)_2$ to Decimal, iv) $(128)_{16}$ to Binary,

   v) $(29.25)_{10}$ to Decimal, vi) $(101101)_2$ to BCD,

   vii) $(101001)_{BCD}$ to Binary, viii) $(A58)_{16}$ to Decimal,

   ix) $(111011)_2$ to gray x) $(101110)_{gray}$ to Binary

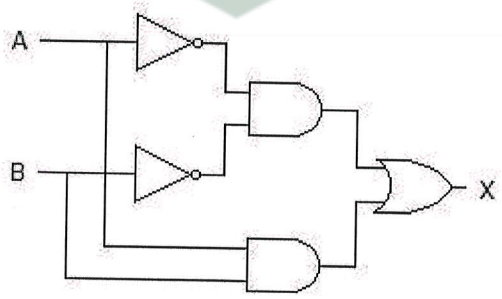
   b) Perform binary subtraction. 2 + 2 = 4

   i) $(14)_{10} - (10)_{10}$ ii) $(21)_{10} - (25)_{10}$

   c) Name the Universal gates. Explain with an example why these are called Universal gates. 4

   d) Implement a NOT gate using an EX-NOR gate. 2

2. a) 5



For the logic circuit diagram above, write its output expression and find out the truth table.

b) A digital circuit has three input lines and one output line such that the output goes HIGH if any two or more input lines are LOW. Find out the truth table, output expression and draw the logic circuit diagram by using minimum number of gates. 5

c) Prove that- 3 X 2 = 6

i) $X.(X+Y)=X$ ii) $(\overline{X}+Y).Y=X.Y$

iii) $(A+B).(A+\overline{B})=A$

d) Minimize the following Boolean Expressions- 2 + 2 = 4

i) $Y=\bar{A}.B.C+A.\bar{B}.C+A.B.\bar{C}+A.B.C$

ii) $Y=(A+B+\overline{C})(A+B+C)(\overline{A}+B+C)$

3. a) Minimize using K-Map technique write the final expression- 4 + 6 = 10

i) $F(A,B,C)=m(0,1,2,6,7)$

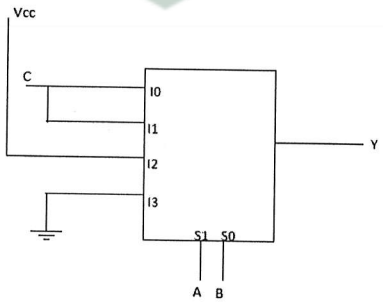
ii) $F(A,B,C,D)=m(4,5,6,7,12,13,14,15)+d(0,1,11)$

b) Explain the working of a half-adder circuit with the help of its truth table and logic diagram. 4

c) Explain the working of a 4-bit binary adder with proper block diagram. 6

4. a) Explain the working of a 4:1 Mux. 6

b) 4



For the 4:1 Mux shown above, find the output expression for Y.

c) Explain the working of a 3-to-8-line Decoder. 6

d) Implement a full-adder with a 3-to-8-line decoder and a few additional gates. 4

5. a) Explain the working of an Active-Low S-R Latch. 5

b) Convert a J-K flip-flop to a D-flip-flop. 5

c) What is a counter? Explain the working of a 3-bit asynchronous ripple counter with proper timing diagram. 2 + 8 = 10