

Total number of printed pages:4

2021

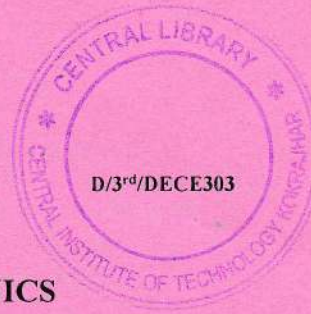
DIGITAL ELECTRONICS

Full Marks: 100

Time: Three hours

The figures in the margin indicate full marks for the questions.

Answer any five questions



Q.1

- a) 1X6=6
- i) Convert decimal 30 into binary number.
 - ii) Simplify $a + ab$.
 - iii) Draw symbol of a XNOR gate.
 - iv) Draw logic diagram of $Y = a+b+c$ using 2 input AND gate only.
 - v) Which gates are called universal logic gates?
 - vi) For a S-R latch if $S=1$ $R=0$ then expected Q output is
- b) 3X2=6
- i) Simplify $x + xy + xyx + xyz + x' + x$
 - ii) Construct the truth table of $Y = a+bc'$
 - iii) Prove that $(x+y)' = x'.y'$
- c) Design a Half adder. 4
- d) Simplify $\sum m(0,1,2,3,4,8,9,10,11)$ using k-map method. 4

Q.2

- a) State whether the following statements are TRUE/FALSE. 1X6=6
- i) $(a + b + c)' = a' + b' + c'$
 - ii) $1 + wxyz + abcd = 1$
 - iii) $x + abc = (x+a)(x+b)(x+c)$
 - iv) $(a' + b' + c' + d)' = a + b + c + d$
 - v) If both the inputs of a NAND gate is 0 then expected output is logic 1.

vi) K-map is a pictorial method of simplifying Boolean equations.

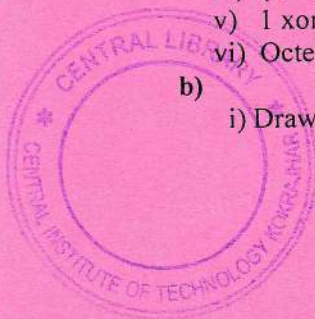
- b) 2X3=6
- i) Convert $xy + yz$ into canonical SOP form .
 - ii) Convert $x(x+y)'$ into Canonical POS form.
 - iii) Write down truth table of a half subtractor.
- c) Simplify $x'yz + xy'z + xyz' + x'yz' + x'y'z'$ using k-map method. 3
- d) Design a Full adder . 5

Q.3 1X6=6

- a) Fill in the blanks.
- i) Number of output for a 4 to 16 decoder is
 - ii) Number of control input needed to design a 4:1 multiplexer is
 - iii) For a 1 : 16 de-multiplexer no of data input is
 - iv) for a half subtractor (a-b) if we apply a=0 b=1 then expected outputs are subtracted output =... Borrow output=....
 - v) Full adder adds number of bits simultaneously .
 - vi) Two NOT gate connected back to back works as bit latch.
- b) 2+3=5
- i) Write down the function table of a 4:1 Multiplexer.
 - ii) Use basic gate to realize $Y = a(b+c)' + a'b'(bc)'$ without changing boolean equation.
- c) Explain S-R latch function with help of it's logic diagram and truth table. 4
- d) Design a 2 to 4 decoder. 5

Q.4 1X6=6

- a)
- i) Convert binary 10011 into decimal.
 - ii) For $j=0$ $k=1$ expected output of j-k latch is
 - iii) Perform binary addition $111 + 101$.
 - iv) $(1 + 0 + 1 + 1)'$ =
 - v) $1 \text{ xor } 0 \text{ xor } 1 \text{ xor } 1 = \dots$
 - vi) Octet is a adjacency of number of 1 inside k map.
- b) 2+2+2 =6
- i) Draw the block diagram of a 1:32 De-multiplexer.



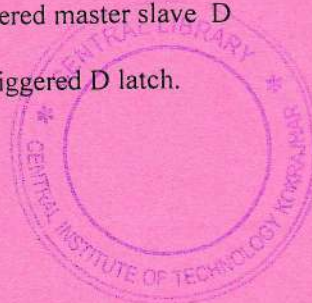
- ii) Write down function table of a J-K latch.
- iii) Use only NAND gate to realize $Y=ab+c$
- c) Simplify $xy'z + xy'z' + x'yz + x'yz' + x'y'z + x'y'z'$ using Boolean algebraic techniques. 4
- d) Simplify $\sum m(4,5,6,7) + d(2,3,8)$ using k-map method. 4

Q.5

- a) 6X1=6
 - i) $00 \rightarrow 01 \rightarrow 11 \rightarrow 01$ is a code sequence.
 - ii) Maxterm for $x=1, y=1, z=1$ is
 - iii) Minterm for $x=1, y=0, z=1$ is
 - iv) Boolean equation of a 4 input(A,B,C,D) XOR gate is
 - v) Applying duality principle on $x.0=0$ results
 - vi) Undefined state of a s-r latch can be removed by replacing s-r latch with latch.
- b) 2+2+2=6
 - i) Write down the function table of a 4 to 2 encoder.
 - ii) Simplify $(1+0)' + 0 + (1.1)' + (x'+y'+z)'+(xyz)'$
 - iii) Draw logic diagram of $Y = a+b'+cd$
- c) 6+2=8
 - i) Draw block diagram of master slave flip flop using D-latch symbol, NOT gate and explain it's operation.
 - ii) Draw the logic diagram of a S-R latch with enable.

Q.6

- a) 5+5=10
 - i) Describe general steps to design a combinational circuit.
 - ii) Describe the procedure of simplifying a Boolean equation using k-map method.
- b) 6+1+1+2=10
 - i) Describe function of pulse triggered latch with the help of logic diagram, timing diagram etc.
 - ii) Write down truth table of a OR gate.
 - iii) Draw the symbol of a Negative edge triggered master slave D latch.
 - iv) Write down truth table of negative edge triggered D latch.



Q.7

a)

10 +6=16

i) Describe the function of 2 bit asynchronous counter with block diagram, timing diagram, table to show count status etc.

ii) Design a 1:8 De-Multiplexer.

b)

3+1=4

i) Distinguish between combinational and sequential circuit.

ii) Subtract 10000 - 111 .

