Total number of printed pages:4

D/3rd/DECE302

2021

ELECTRONIC DEVICES AND CIRCUITS

Full Marks: 100

Time: Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. a) The number of electrons in the valence shell of Si is _____. 1

   b) The unit of resistivity is _____. 1

   c) At zero degree Kelvin, the acceptor energy level is completely _____. 1

   d) In a semiconductor, the product of electron and hole concentrations is a constant of _____. 1

   e) Under reverse bias, the current in a p-n junction diode is due to _____ carriers. 1

   f) The expression for forward bias current can be approximated as _____ function. 1

   g) The dynamic resistance of a diode varies with the _____ of the diode. 1

   h) The voltage across a Zener diode is _____when it is operating in the breakdown region. 1

   i) An LED emits light when it is _____ biased. 1

   j) If we connect a Si and Ge diodes in parallel (with same type of bias) and them in series with a 100-ohm resistance and a battery of 1Volts, the current will flow through _____ diode. 1

   k) The peak inverse voltage (PIV) rating required for the diode used in half wave rectifier (HWR) circuit is _____. 1

   l) The conduction angle for a full wave rectifier (FWR) with ideal diodes is _____ degrees. 1

   m) The average dc voltage at the output of a FWR with ideal diodes is _____ times that of a HWR. 1

n) In a clamper circuit which can shift the input waveform upwards, the capacitor voltage will have a polarity in the _____ direction of the input waveform. 1

o) The regulation of output voltage against the variation of input fluctuation is called _____. 1

p) The _____ region has the smallest width in the structure of BJT. 1

q) The dc current gain in CB configuration is approximately equal to _____. 1

r) For obtaining the ac equivalent circuit, the dc voltage sources are replaced by _____. 1

s) For common collector (CC) configuration, the load resistance is connected to _____ terminal of the transistor. 1

t) The gate material in a p-channel JFET is made of _____. 1

2. a) Why the number free electrons and holes are equal for intrinsic semiconductor? 4

b) What do you understand by the term 'doping'? 4

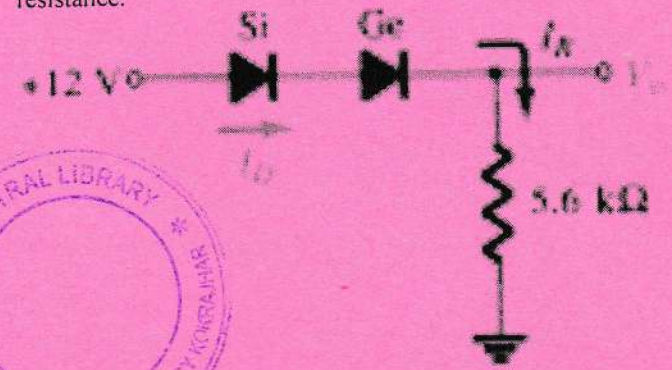
c) Draw the energy band diagram of n-type and p-type semiconductors and discuss why they have greater conductivity than the intrinsic semiconductor. 8

d) What do you mean by depletion region and how it is created in a p-n junction diode? 4

3. a) Draw and explain the I-V characteristics of a p-n junction diode. 4

b) Discuss the mechanism of avalanche breakdown in a reverse biased p-n junction diode. 4

c) In the following circuit, find the value of current through 5.6KΩ resistance. 4



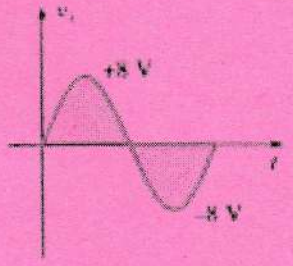
d) Draw the diode-resistor circuit implementation of a two input OR gate and explain how it satisfies the truth table. 4

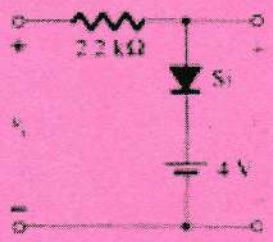
e) Draw the circuit diagram of a center tapped transformer FWR and explain its working. 4

4. a) Derive the value of minimum input voltage required for regulation action in a Zener voltage regulator. 5

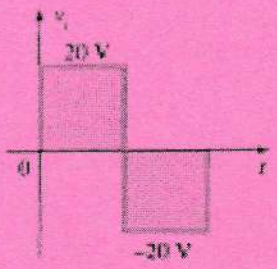
b) Why Bipolar Junction Transistor (BJT) is called so? Explain the working of a BJT biased in an active mode. 5

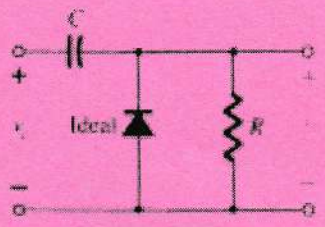
c) Find the output voltage waveform of the following circuit. 5





d) Identify the following circuit and plot its output waveform. 5



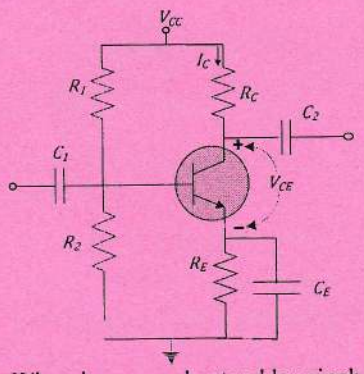


5. a) Draw the circuit diagram of a pnp transistor biased under CB configuration and mark the direction of current flow at each terminal. Identify the input and output current and voltages for this configuration. 5

b) Draw the input and output characteristics of a BJT in CE configuration and explain how it is able to amplify a weak input signal. 5

c) Explain the purpose of biasing circuits in small signal amplifiers. 4

d) Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider bias network shown below. 6



Given
$\beta = 100$, V_{CC}=+22.0V,
$R_1 = 39K\Omega$, $R_2 = 3.9K\Omega$,
$R_E = 1.5K\Omega$, $R_C = 10K\Omega$,
$C_E = 50\mu F$ and
$C_1 = C_2 = 10\ \mu F$

6. a) What do you understand by pinch-off in JFET operation? Explain how it differs when V_{GS}=0 in comparison to when V_{DS}=0. 5

b) Write the expression for saturation current for a p-channel JFET as a function of gate to source voltage and explain its significance. 5

c) Draw the schematic diagram of a p-channel depletion type MOSFET and explain its working. 5

d) Write the expression for transfer characteristics of an enhancement type MOSFET. Explain how it could be used to explain the operation of both n-channel and p-channel devices. 5

7. a) Draw the r_e model of a BJT in CE configuration and explain how it is able to duplicate its small signal operation. 6

b) Write the hybrid parameter equations for a two-port network. Discuss what each parameter stands for when it models a BJT in CB configuration. 6

c) Derive the expressions for (i) input impedance Z_i (ii) output impedance Z_0 and (iii) voltage gain A_V in the case of a voltage-divider bias network using its small-signal equivalent. 8