Total number of printed pages: 3

D/3rd/DCSE301

2023

COMPUTER ARCHITECTURE AND ORGANIZATION

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1.	a)	Draw the hardwired control unit of a basic computer and explain each component in brief.				6
	b)	A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.				6+4=10
		i)	How many bits are there in the operation code, the register code part and the address part?			
		ii)	Draw the instruction word format and indicate the number of bits in each part.			
	c)	Write the functions of AR and IR.				2+2=4
2.	a)	Draw the flowchart of an instruction cycle and discuss each phase in brief.				10
	b)	Write the register transfer statements corresponding to the micro-operations executed for the following instructions.				5x2=10
		i)	CIR	(iv)	BSA	
		ii)	SZA	(v)	SKI	
		iii)	LDA			
3.	a)	What to do you mean by a program interrupt? Demonstrate the interrupt cycle with the help of an example.				2+6=8
	b)	Write a program to evaluate the following arithmetic statement X=(A+B)*(C+D)				4x3=12
		i)	Using a general register computer with three address instructions			

		ii)	Using a general register computer with two address instructions.			
		iii)	Using an accumulator-type computer with one address instructions.			
		iv)	Using a stack-organized computer with zero address instructions.			
4.	a)	What do you mean by addressing mode of an instruction?				3
	b)	Discuss any 3(three) types of addressing modes in brief.				3x3=9
	c)	An instruction is stored at location 300 and its address field is at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is				4x2=8
		i)	direct	iii)	relative	
		ii)	immediate	iv)	register indirect	
5.	a)	Consider a typical 128 x 8 RAM chip.				4+2+4+2=12
		i)	Show the block diagram and explain in brief.			
		ii)	How many such RAM chips are needed to provide a memory capacity of 2048 bytes?			
		iii)	How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?			
		iv)	Mention the number of lines to be decoded for chip select input in order to select each of these RAM chips?			
	b)	Define locality of reference.				2
	c)	Discuss about write-through and write-back cache policies.				3+3=6
6.	a)	A two-way set associative cache memory can accommodate a total of 2048 words from main memory. The main memory size is 128Kx32.				6+2=8
		i)	Formulate all information required to construct the cache memory.			
		ii)	What is the size of the cache memory?			
	b)	State the differences between isolated I/O and memory-mapped I/O.				5

	c)	What is the basic advantage of using interrupt-initiated data transfer over transfer under program control without an interrupt?	3
	d)	Write a brief note on – DMA	4
7.	Write short notes on any four(4) of the following:		4x5=20
	a)	Stored program concept	
	b)	Status bit conditions	
	c)	Memory hierarchy	
	d)	Virtual memory	
	e)	Input-output interface	